JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST-3 EXAMINATION-June 2023

M.Tech-II Semester (ECE)

COURSE CODE (CREDITS): 21M11EC211 (3) MAX. MARKS: 35

COURSE NAME: Digital System Design using Verilog HDL

COURSE INSTRUCTOR: Dr. Pardeep Garg MAX. TIME: 2 Hours

Note: (a) All questions are compulsory. (b) Marks are indicated against each question in square brackets. (c) The candidate is allowed to make suitable numeric assumptions wherever required for solving problems.

Q1. A Verilog design module code is written as follows:

```
reg [8:0] flag;
integer i;
initial
begin
        flag = 8'b 0001_0000;
        j=0;
        begin: block1
        while (j<8)
            begin
                if (flag[j])
                    begin
                        $display("Encountered a True bit at position %d", j);
                        disable block1;
                    end
                j=j+1;
            end
    end
end
```

i) Emphasizing on the special feature of block, discuss the functioning of the above Verilog code achieved w.r.t the special feature.

ii) If similar kind of program has to be written in C language, the special feature of block highlighted here will be replaced by which feature option available in C language? Also, compare the functioning of Verilog language and C language w.r.t this feature.

[CO-3, 2.5+2.5=5 marks]

Q2(i). C is a sequential language whereas Verilog HDL is a concurrent language. Justify the concurrent nature of Verilog HDL language with the help of a programming example which uses multiple initial statements and show the output also.

[CO-1, 4 marks]

Q2 (ii). Clock is a recurring pattern pulse. A clock has to be generated of time period 30 time units which is initialized at time zero and the simulation should finish in 1200 time units. Write a Verilog design code module for the same. **[CO-1, 3 marks]**

Q3. Blocking and Nonblocking assignments can be used in Verilog modules, differentiate between these two by discussing their execution style, operator used etc by taking suitable example. Out of these two, which one is preferred in digital design and why? Which assignment out of these suffers from race condition and which one does not suffer, discuss using a suitable example. **[CO-2, 2+1+2=5 marks]**

Q4. Employing suitable example of each, discuss the usefulness of *forever* and *repeat* loop in Verilog HDL. **[CO-2, 2+2=4 marks]**

Q5. It is said that in some situations *while* loop is appropriate and in some situations *for* loop is more appropriate to be used. Justify this statement with proper logic and test cases for both loops. **[CO-2, 1.5+1.5=3 marks]**

Q6. How is the sensitivity list/event OR control defined and used in Verilog HDL? Discuss with different test cases (with variable number of inputs). **[CO-2, 3 marks]**

Q7. The use of if-else loop is generally preferred in conditional statements. The if-else-if loop can be nested also. But the nested if-else-if loop can become unwieldy if there are too many alternatives. What is the appropriate statement to be preferred in this situation? Discuss that statement employing a suitable example in Verilog HDL. **[CO-2, 4 marks]**

Q8(i). '*In Verilog, if there are no timing control statements, the simulation time does not advance*' justify the use of timing controls in Verilog in context of this statement. **[CO-4, 1 mark]**

Q8(ii). Discuss the use of regular delay control, intra-assignment delay control, and zero delay control using suitable example for each. **[CO-4, 3 marks]**