JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -3 EXAMINATION- 2023

B.Tech- **VI** Semester (**ECE**)

COURSE CODE (CREDITS): 18B11EC612 (3) MAX. MARKS: 35

COURSE NAME: VLSI Technology

COURSE INSTRUCTORS: Dr. Harsh Sohal MAX. TIME: 2 Hours

Note: *(a)All questions are compulsory.*

(b)Marks are indicated against each question in square brackets.

(c) The candidate is allowed to make Suitable numeric assumptions wherever required for solving problems

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Q1. [CO1+CO2][7]

(a)Why the input resistance of a CMOS inverter is infinite? [1]

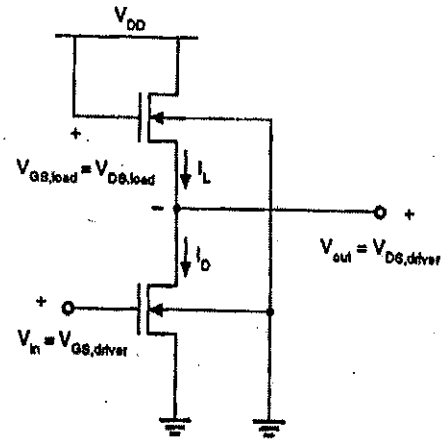
(b) List the differences between BJT and MOSFET. [2]

(c) Explain the formation of Inversion layer in an n channel MOSFET (use diagrams). [2]

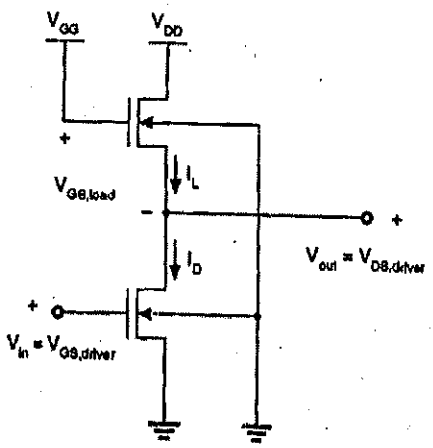
(d)You are given a wafer of the size of 30 cm, die size of 2.5 cm2, with 1 defects/cm2; α (the measure of manufacturing process complexity)=3. Cost of the wafer is INR 100,000. Calculate: (i) dies per wafer (ii) die yield [1+1]

Q2. [CO2+CO3] [7]

For the inverter circuits given below derive the expression for V_{OH} for both (a) and (b). Which of the two shall give better output voltage swing? Explain. [3]



(a)



(b)

(b) [2+2]

For the circuit in Figure (b) above list the region of the operation of the load transistor and the driver transistor for the following values of I/P and O/P voltages.

Vin	Vout	Driver Operating Region	Load Operating region
V_{OL}	V_{OH}	?	?
V_{IL}	$\approx V_{OH}$	?	?
V_{IH}	Small (slightly greater than V_{OL})	?	?
V_{OH}	V_{OL}	?	?

Q3. [CO3+CO4] [8]

(a)Given V_{DD} = 2.5 V, k' = 40μA/V^2, andV_{T0}= 0.5 V, design a resistive-load inverter circuit with V_{OL}= 0.1 V.

(i) Determine the (W/L) ratio of the driver transistor and the value of the load resistor R_L that achieves the required V_{OL}. [3]

Calculate the DC power dissipation of the inverter above (assuming that the input voltage is "low" during 50% of the operation time, and "high" during the remaining 50%) when W/L=1. [1]

(b) Consider a CMOS inverter circuit with the following parameters: [2+2]

V_{DD} =5V

$V_{T0,n}$ = 1 V

$V_{T0,P}$= -1 V

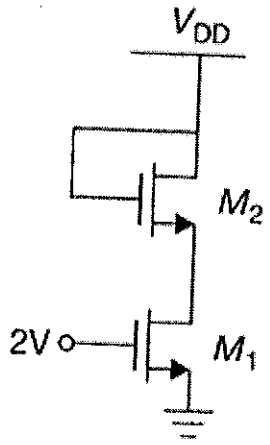
k_n= 200 μA/V^2

k_p = 80 μA/V^2

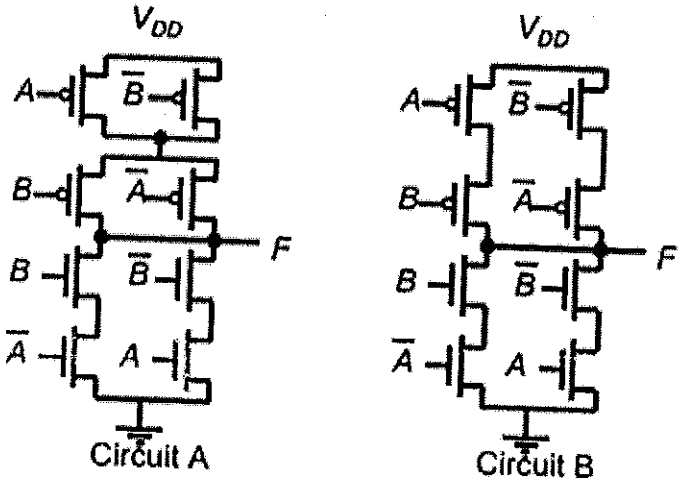
Calculate (i) Noise Margin Low (NM_L) (ii) Threshold voltage (V_{TH}) of the CMOS inverter

Q4. [CO5, CO6][6]

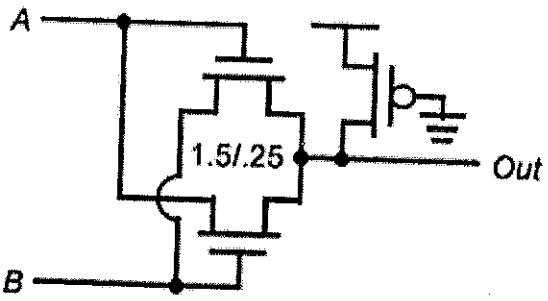
(a) Calculate the minimum supply voltage (V_{DD} in Volts) required for the transistor M1 to operate in saturation mode. Consider the following quantities given for the nMOS: K_n = $\mu_n C_{ox}(W/L)$ =1mA/V^2; V_{THN} =1.9V both the transistors. Assume that the channel length modulation is zero and the body is shorted to the source.[2]



(b) Write the Boolean equations being implemented by the circuits given below.(1+1)



(c) What is the logic being implemented by the circuit below? What is the logic style used? List its comparison with static CMOS logic implementation. [2]



Q5. [CO5, CO6] [7]

(a) Implement the Boolean function F=$\overline{(D+E+A)(B+C)}$ using static CMOS logic and draw the corresponding circuit diagram. [2]

(b) Find an equivalent CMOS inverter circuit for the above implementation in (a) for simultaneous switching of all inputs, assuming that $(W/L)_p = 15$ for all pMOS transistors and $(W/L)_n = 10$ for all nMOS transistors. [2]

(c) Determine the Boolean function being implemented by the following Transmission gate implementation while writing intermediate equations. [3]