JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -3 EXAMINATION- 2023

B.Tech- VIII Semester (ECE)

COURSE CODE(CREDITS): 19B1WEC831(3) MAX. MARKS: 35

COURSE NAME: Digital CMOS ICs

COURSE INSTRUCTORS: Dr. Harsh Sohal MAX. TIME: 2 Hours

Note: ***(a)*** *All questions are compulsory.*

(b)Marks are indicated against each question in square brackets.

(c) The candidate is allowed to make suitable numeric assumptions wherever required for solving problems

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Q1. [CO1+CO2][8]

(a) Why MOSFETs are call as the field effect Transistors? Describe. [1]
(b) What is the polarity of the inversion layer in an n type MOSFET and a p Type MOSFET? [1]
(c) In order to avoid substrate bias where do we connect the substrate terminal of nMOS and pMOS devices? [1]
(d) Why do MOSFET circuits consume less power than BJT based circuit implementation? [1]
(e) What is feature size in CMOS technology? How can we relate it to minimum size devices? [2]
(f) What are the macroscopic design challenges in VLSI? How can they be managed? [2]

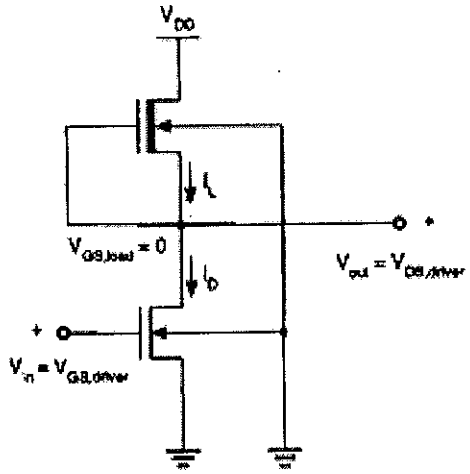
Q2.[CO2+CO3] [8]

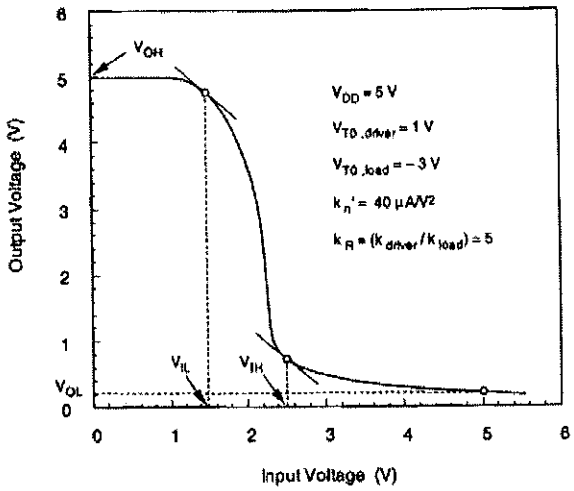
(a) Explain the construction and working of an Enhancement type n-MOSFET with suitable diagrams while defining inversion layer, suitable equations of current flow etc. How does it differ from Depletion MOSFET? (Explain on the basis of construction and working) [4]

(b) For the circuit and the VTC given below find out what will be the region of the operation of the load transistor and the driver transistor for the following values of I/P and O/P voltages. [2+2]

Also find out the threshold voltage of the inverter.

Vin	Vout	Driver Operating Region	Load Operating region
V_{OL}	V_{OH}	?	?
V_{IL}	$\approx V_{OH}$	?	?
V_{IH}	Small (slightly greater than V_{OL})	?	?
V_{OH}	V_{OL}	?	?
V_{TH}	V_{TH}	?	?





Q3 [CO3+CO4] [8]

(a)Consider a resistive-load inverter circuit with V_{DD}= 5 V, k '=$\mu_n C_{ox}$ =20 $\mu A/V^2$, V_{T0}= 1 V, R_L = 200 kW, and W/L = 3. Calculate the critical voltages (V_{OL}, V_{OH}, V_{IL}, V_{IH}) on the VTC.

Also find the noise margins of the circuit. (Draw the required inverter circuit and VTC curve. You may derive expressions and then use them). [4]

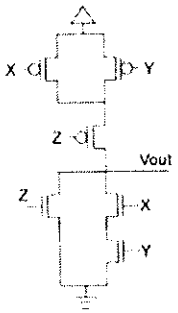
(b) Consider a CMOS inverter circuit with the following parameters: [2+2]

V_{DD} =5V ; $V_{T0,n}$ = 1 V; $V_{T0,P}$= -1 V; k_n= 200 $\mu A/V^2$; k_p = 80 $\mu A/V^2$

Calculate (i) Noise Margin Low (NM_L) (ii) Threshold voltage (V_{TH}) of the CMOS inverter

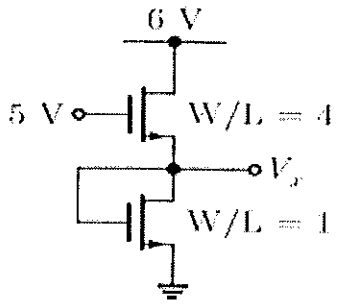
Q4.[CO4+CO5][4]

(a) For the circuit given below



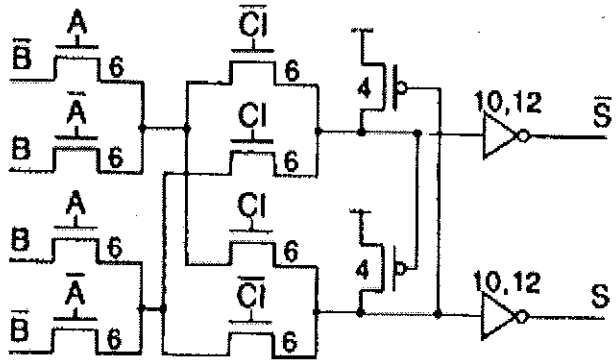
(i) identify the Boolean function being implemented (ii) Implement the function obtained in (i) using nMOS devices only. [2]

(b) In the circuit below for the MOS transistors $\mu_n C_{ox}$ =100μ/A/V^2 and the threshold voltage VT=1V. Find out the voltage V_x as for the figure below. [2]



Q5. [CO4+CO5] [3+4]

(a) Determine the Boolean function being implemented by the following Complementary Pass Transistor Logic (CPL) gate implementation while writing intermediate equations. [3]



(b) Implement the Boolean function F=$\overline{(\ ABC + A\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}\bar{C}B)}$ using static CMOS logic and draw the corresponding circuit diagram. [2]

Find an equivalent CMOS inverter circuit for the above implementation in for simultaneous switching of all inputs, assuming that $(W/L)_p = 15$ for all pMOS transistors and $(W/L)_n = 10$ for all nMOS transistors. [2]