JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST-3 EXAMINATION- MAY-2023

B.Tech-VIII Semester (ECE)

COURSE CODE (CREDITS): 19B1WEC832 (3) MAX. MARKS: 35

COURSE NAME: CAD Algorithms for Synthesis of Digital Systems

COURSE INSTRUCTOR: Dr. Pardeep Garg MAX. TIME: 2 hours

Note: All questions are compulsory. Marks are indicated against each question in square brackets. CO indicates Course Outcomes.

Q1(i). Obtain binary decision diagram (BDD) for the function (F) by following the variable expansion sequence as a>b>c:

$$F(a,b,c) = a.b + \bar{a}.c + a.\bar{b}.c$$ [CO-4, **2.5 marks**]

Q1(ii). Does the variable ordering for expansion in BDD affect the size of BDD? Discuss with the help of a suitable example. [CO-4, **1.5 marks**]

Q1(iii). What are the basic rules which are followed in reducing the size of BDD to obtain ROBDD. Obtain the ROBDD structure of the result obtained in **Q1(i)**. [CO-4, **3 marks**]

Q1(iv). One of the applications of BDDs is in the synthesis of systems. In this context, show the realization of result obtained in Q1(iii) part using 2:1 multiplexers. [CO-4, **2 marks**]

Q2(i). Why is decomposition of any given function done? Discuss the functioning of Ashenhurst, Curtis, and non-disjoint decomposition with a suitable example for each of these.

[CO-4, **0.5+1+1+1=3.5 marks**]

Q2(ii). Compute the Boolean decomposition using Ashenhurst, Curtis decomposition for the following function: $F(a,b,c,d) = a.\bar{b}.\bar{c}.\bar{d} + a.\bar{b}.c.d + \bar{a}.b.\bar{c}.\bar{d} + \bar{a}.b.c.d + a.b.\bar{c} + \bar{a}.\bar{b}.\bar{c}$ [CO-4, **3.5 marks**]

Q3. Discuss the term Fusion in the context of graph theory. Obtain the fused graph corresponding to vertices a, and b in the **Figure 1**: [CO-2, **1+1=2 marks**]

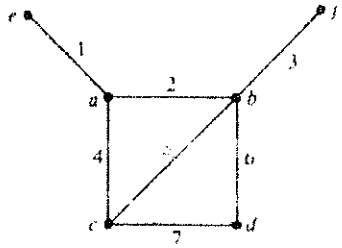

Figure 1

Q4. Compute the minimal expression using Quine-McCluskey method for the following expression:

$$f = \sum m(1, 2, , 3, 5, 6, 7, 8, 9, 12, 13, 15)$$ **[CO-2, 5.5 marks]**

Q5. Discuss the concept of false path in VLSI employing suitable examples of multiplexer and flip-flop. [CO-5, 3 marks]

Q6. Discuss the concept of retiming w.r.t. delay in digital systems. [CO-5, 3 marks]

Q7. Why minimization of sequential circuits is required? Obtain the state table, reduced state table, reduced state diagram for the state machine whose state diagram is shown in **Figure 2**.

[CO-5, 1+1.5+1.5+1.5=5.5 marks]

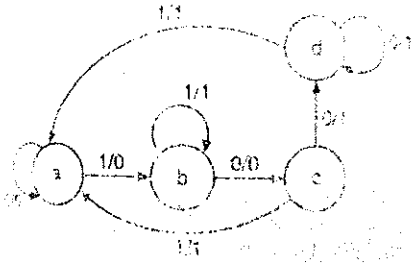

Figure 2