JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST-2 EXAMINATION-MAY-2023

M.Tech-II Semester (ECE)

COURSE CODE (CREDITS): 21M11EC211 (3) MAX. MARKS: 25

COURSE NAME: Digital System Design using Verilog HDL

COURSE INSTRUCTOR: Dr. Pardeep Garg MAX. TIME: 1 Hour 30 Minutes

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Note: All questions are compulsory. Marks are indicated against each question in square brackets. CO indicates the Course Outcomes.

Q1. Compute the result of the following operations in Verilog HDL:

a) Z=m**n for m=6, n=3 **b)** out=A>>2 for value of A=4'b0011

c) ^A for the value of A= 5'b10010 **d)** Y=(2{P} , 5'b110, 4{Q}) for P=2'b01, Q=1'b1

e) –'d20/10 **vi)** Z=!Y for Y=5 **[CO- 2, 1*6=6 marks]**

Q2. The logical equality operators when operated on operands can yield an unknown (x) value whereas the case equality operators yield either 1 or 0 but never an unknown (x) value. Prove this statement using suitable examples. **[CO-2, 2.5 marks]**

Q3. Discuss in detail the significance and increasing popularity of data flow modeling over gate-level modeling. **[CO-2, 2 marks]**

Q4. How is the conditional/ternary operator used in Verilog HDL? Discuss assuming any appropriate example by writing a Verilog code (design code only) in data flow modeling.

[CO-2, 1+2=3 marks]

Q5. Two signals X and Y are given as input to an OR gate. Input A is low initially, goes high at 10 units of time and then goes low at 70 units of time; input B is alternately low and high for 10 units of time each (total time duration is 90 units). Draw the output waveform w.r.t. output variable Z for the condition given in the following Verilog statement:

assign #5 Z= A | B;

[CO-2 , 2.5 marks]

Q6. Distinguish between the working and the corresponding result obtained for bitwise and logical operators employing sufficient test cases. **[CO-2, 2.5 marks]**

Q7. Why the ports of type input and inout cannot be declared as *reg*? Discuss with suitable justification. **[CO-2, 1.5 marks]**

Q8. An 8:1 multiplexer has to be designed. Draw the logic diagram of the circuit for this situation. Write the gate-level modeling based Verilog design code corresponding to your logic diagram. **[CO-3, 1.5+3.5=5 marks]**