JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -1 EXAMINATION- FEB-2023

COURSE CODE (CREDITS): 19B1WEC831 (3) MAX. MARKS: 15

COURSE NAME: Digital CMOS ICs

COURSE INSTRUCTORS: Dr. Harsh Sohal MAX. TIME: 1 Hour

Note: *All questions are compulsory. Marks are indicated against each question in square brackets.*

Q1. [CO1][6]

(a)Explain the construction and working of a Depletion type MOSFET with suitable diagrams while defining inversion layer, suitable equations of current flow etc. [3]

(b)List the differences between BJT and MOSFET. Which of the two is preferred for VLSI design and why? [2+1]

Q2. [CO1][6]

(a) What is noise margin? How it adds to noise immunity? [2]
(b) For a given inverter the V_{OH}=0.9V; V_{OL}= 0.1V; V_{IL} = 0.2V; V_{IH}=0.8V. Calculate Noise Margins, NM_L and NM_H.[1]
(c) Explain the terms Power-Delay-Product (PDP) and Energy-delay product (EDP) (with mathematical expressions). Which of the two is a better design metric for IC designing? Justify with reason(s) .[3]

Q3. [CO1] [3]

(a) What are the macroscopic design challenges in VLSI? How can they be managed? [2]
(b) In the Figure below are the Transfer characteristics of a BJT or an E MOSFET or a D-MOSFET or a JFET.[1]