JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -1 EXAMINATION- FEB-2023

COURSE CODE(CREDITS): 18B11EC411 (03) MAX. MARKS: 15

COURSE NAME: ANALOG INTEGRATED CIRCUITS

COURSE INSTRUCTORS: Dr. Shruti Jain MAX. TIME: 1 Hour

Note: All questions are compulsory. Marks are indicated against each question in square brackets.

SHORT ANSWERS (1 × 5 = 5 marks)

1.

a) Assume that an operational amplifier has I_{B1} = 300nA and I_{B2} = 250nA. Determine the average bias current.

b) If Sita is going for AC analysis, than what values she is evaluating.

c) Prove Common Mode Rejection Ratio is ideally infinite.

d) Shyam wants to write an output voltage equation, in terms of differential input voltage and common mode voltage. Help him in writing the same.

e) Why current mirror and constant current bias differential amplifier circuits are preferred over the resistive differential amplifier circuits.

[CO1, CO2]

LONG ANSWERS (2 × 5 = 10 marks)

2. Ram is studying the effect of Darlington pair. He has replaced the transistors of emitter biased dual input balanced differential amplifier with Darlington pair. Show the effect on *input resistance* if he uses (a) normal transistor and (b) Darlington pair. Assume the following specifications: $V_{CC} = 10V$, $-V_{EE} = -10V$, $R_C = 2.7K\Omega$, $R_{in1} = Rin_2 = 50\Omega$, $R_E = 3.9K\Omega$, $V_{BE} = 0.715V$, $\beta_{ac} = \beta_{dc} = 100$. [CO1]

3. Design the single input balanced output differential amplifier uses diodes constant current bias circuit to meet the following specifications :current supplied by the constant current bias is 4mA, Gain = 40±10, Supply Voltage $V_S = \pm 10V$ [CO2]