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JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -1 EXAMINATION- February 2018

B.Tech VIth Semester

COURSE CODE: 10B11CI613 MAX. MARKS:15

COURSE NAME: Computer Organization and Architecture

COURSE CREDITS: 4 MAX. TIME: One Hr.

Note: *All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means.*

Que-1: ***[05 Marks]***

a. Differentiate Computer organization and computer architecture with an example.
b. Name four techniques used for performance improvement in contemporary computers.
c. What are the possible obstacles to increase of Clock Speed and Logic Density in performance improvement?
d. Differentiate between hardwired controlled system and Programmed controlled system?
e. Define the various classes of interrupts?

Que-2: ***[05 Marks]***

Consider the execution of a program which results in the execution of 2 million instructions on a 400-MHz processor. The program consists of four major types of instructions. The instruction mix and the CPI for each instruction type are given below based on the result of a program trace experiment:

Instruction Type	CPI	Instruction Mix
Arithmetic and Logic	1	60%
Load/Store with cache hit	2	18%
Branch	4	12%
Memory reference with cache miss	8	10%

Now assume that the program can be executed in eight parallel tasks or threads with roughly equal number of instructions executed in each task. Execution is on an 8-core system with each core (processor) having the same performance as the single processor originally used. Coordination and synchronization between the parts adds an extra 25,000 instruction executions to each task. Assume the same instruction mix as in the table for each task, but increase the CPI for memory reference with cache miss (searched information is not available in cache) to 12 cycles due to contention for memory.

a. Determine the average CPI.
b. Determine the corresponding MIPS rate.
c. Calculate the speedup factor.
d. Compare the actual speedup factor with the theoretical speedup factor determined by Amdhal's law.

Que.3: ***[05 Marks]***

a. What are the possible methods of timings of the bus operations? Explain and provide the timing diagram for each one.
b. Describe the QPI four-layer protocol architecture in detail. Also explain the multilane distribution of flits to phits with proper diagram.