Dr Hem Raj

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JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT
TEST -III EXAMINATION- May 2018
B.Tech VIth Semester

COURSE CODE: 10B11CI613 MAX. MARKS: 35
COURSE NAME: Computer Organization and Architecture
COURSE CREDITS: 4 MAX. TIME: 2Hrs

Note: All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means.

Que.1: ***[CO3; 5 Marks]*** Provide the flowchart for Booth's algorithm. Given a = 0011 and b = 1011 in twos complement notation (a =3 and b = -5), compute the product p = a x b with Booth's algorithm.

Que.2: ***[CO3 & CO4; 5 Marks]*** A pipeline with 18 stages runs a program P having 4,076 instructions. Branches comprise 17 percent of the instructions, and the "branch not taken" assumption holds for branch prediction. Further assume that 41 percent of the branches are predicted correctly, and there is an average penalty of 1.7 cycles for each mispredicted branch. Additionally, 2 percent of the total instructions incur an average of 1.3 stalls each. Calculate the CPI of P on this pipeline. ***Note***: Show all work to get full credit if your answer is correct, partial credit if not.

Que.3: (A) ***[CO4; 3 Marks]*** Give an example with ***output dependency*** and another one with ***anti dependency***. Show how they can be solved by register renaming.

(B) ***[CO4; 2 Marks]*** Which data dependencies have to be considered by a superscalar CPU using:

- in-oder issue with in-order completion?
- out-of-order issue with out-of-order completion?

Que.4: For all following questions we assume that:

a) Pipeline contains stages: IF (Instruction Fetch), IS (Instruction Issue), RO (Read operand), EX (Instruction Execution) and W (Write Results);

b) Each stage except EX requires one clock cycle;

c) System contains 4 FUs for FP operations, FP-load / store, FP-addition / subtraction FP-multiplication and FP-division;

EX-stage for Load / Store operations contains 1 clock cycle (EX);

EX-stage for ADDD or SUBD operations contains 1 clock cycle (A or S);

EX-stage for MULTD operation contains 3 clock cycles (M1, M2, M3);

EX-stage for DIVD operation contains 4 clock cycles (D1, D2, D3, D4);

d) All memory references hit in cache;

e) Pipeline has forwarding hardware for all FUs, except FP-Load / Store where operand is ready after W-stage;

Timing diagram of task segment processing is presented as below in table-

Instruction	Clock cycle number																
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
LD F6, 20(R5)	IF	IS	RO	EX	W												
LD F2, 28(R5)		IF	IS	RO	EX	W											
MULTD F0,F2,F4			IF	IS	*	*	RO	M1	M2	M3	W						
SUBD F8,F6, F3				IF	IS	RO	S	W									
DIVD F10,F0,F6					IF	IS	*	*	*	*	R0	D1	D2	D3	D4	W	
ADDD F6, F8,F2						IF	IS	RO	A	W							
SD F8, 50(R5)							IF	IS	RO	EX	W						

(A) *[CO5; 3 Marks]* What kind of hazards are between following instructions? Give explanation.

I. LD F2, 28(R5) and MULTD F0, F2, F4
II. DIVD F10, F0, F6 and ADDD F6, F8, F2
III. MULTD F0, F2, F4 and SD F8, 50(R5)

(B) *[CO5; 3 Marks]* What kind of data hazards are between following instructions? Give explanation.

IV. MULTD F0, F2, F4 and DIVD F10, F0, F6
V. DIVD F10, F0, F6 and ADDD F6, F8, F2
VI. MULTD F0, F2, F4 and SD F8, 50(R5)

Que.5: Assume that a superscalar pipeline capable of fetching and decoding two instructions at a time, having three separate functional units (e.g., two integer arithmetic and one floating-point arithmetic), and having two instances of the write-back pipeline stage. The example assumes the following constraints on a six-instruction code fragment:

- I1 requires two cycles to execute.
- I3 and I4 conflict for the same functional unit.
- I5 depends on the value produced by I4.
- I5 and I6 conflict for a functional unit.

Consider the following code fragment and answer the question given below:

I1: R3 d R3 op R5
I2: R4 d R3 + 1
I3: R3 d R5 + 1
I4: R7 d R3 op R4

(A) *[CO5; 2 Marks]* Provide the superscalar Instruction Issue and completion policy for "In-order issue with in-order completion".

(B) *[CO5; 2 Marks]* Provide the superscalar Instruction Issue and completion policy for "In-order issue with out-of-order completion".

(C) *[CO5; 2 Marks]* Provide the superscalar Instruction Issue and completion policy for "Out-of-order issue with out-of-order completion".

Que.6: (A) *[CO6; 2 Marks]* What is the meaning of each of the four states in the MESI protocol?
(B) *[CO6; 2 Marks]* Why there is a trend towards giving an increase fraction of chip area to cache memory?

Que.7: *[CO1 & CO3; 4 Marks]* Consider a disk with N tracks numbered from 0 to (N - 1) and assume that requested sectors are distributed randomly and evenly over the disk. We want to calculate the average number of tracks traversed by a seek.

(A) First, calculate the probability of a seek of length j when the head is currently positioned over track t. Hint: This is a matter of determining the total number of combinations, recognizing that all track positions for the destination of the seek are equally likely.

(B) Next, calculate the probability of a seek of length K. Hint: this involves the summing over all possible combinations of movements of K tracks.

(C) Calculate the average number of tracks traversed by a seek, using the formula for expected value

$$E[x] = \sum_{i=0}^{N-1} i \times \Pr[x = i]$$

(D) Show that for large values of N, the average number of tracks traversed by a seek approaches N/3.