Dr Vivek

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JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -2 EXAMINATION- April 2018

B.Tech IV Semester

COURSE CODE: 10B22CI421 MAX. MARKS: 25

COURSE NAME: Computer Organisation

COURSE CREDITS: 04 MAX. TIME: 1.5 Hrs

Note: *All questions are compulsory. Each question carries equal marks. Carrying of mobile phone during examinations will be treated as case of unfair means.*

1. (a) A computer uses a memory unit with 256 K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit. an operation code, a register code part to specify one of 64 registers, and an address part.
   i. How many bits are there in the operation code, the register code part, and the address part?
   ii. Draw the instruction word format and indicate the number of bits in each part.
   iii. How many bits are there in the data and address inputs of the memory?

   (b) For each of the following 16-bit instructions, give the equivalent four-digit hexadecimal code and explain in your own words what it is that the instruction is going to perform. Give the symbolic representation of each instruction.
   i. 0001 0000 0010 0100
   ii. 1011 0001 0010 0100
   iii. 0111 0000 0010 0000
   iv. 0111 0000 0000 0010
   v. 1111 0000 0100 0000

2. (a) Draw and explain the hardwired Control Unit for the basic computer.
   (b) What are Instruction Cycle Phases? Draw and explain the common bus with timing clock for Instruction cycle: [Fetch Decode [Indirect] Execute] *

   T0: AR ← PC (S0S1S2=010, T0=1)
   T1: IR ← M [AR], PC ← PC + 1 (S0S1S2=111, T1=1)
   T2: D0, . . . , D7 ← Decode IR(12-14), AR ← IR(0-11), I ← IR(15)

3. (a) The memory unit of the basic computer is to be changed to a 65,536 x 16 memory, requiring an address of 16 bits. The instruction format of a memory-reference instruction remains same for I = 1 (indirect address) with the address part of the instruction residing in positions 0 through 11. But when I = 0 (direct address), the address of the instruction is given by the 16 bits in the next word following the instruction. Modify the micro operations during time T_2 T_3 (and T_4 if necessary) to conform with this configuration.

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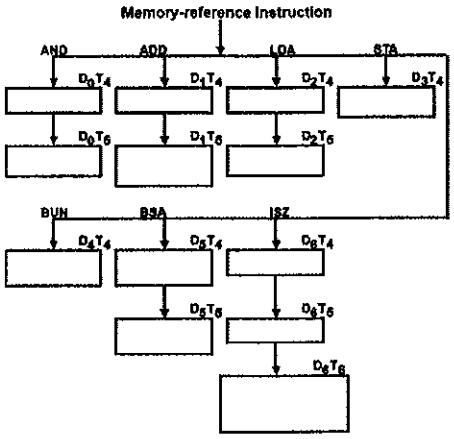
(b) Write RTL for each memory referenced instruction.



4. (a) Specify the RTL for following control inputs, that will be executed during the next clock cycle.

	S_2	S_1	S_0	LD of register	Memory	Adder
a.	1	1	1	IR	Read	-------
b.	1	1	0	PC	-------	------
c.	1	0	0	DR	Write	-------
d.	0	0	0	AC	-------	Add

(b) What is the value of r in Register Reference Instructions? Specify the RTL for following register instructions.

CLA	rB_{11}:
CLE	rB_{10}:
CMA	rB_9:
CME	rB_8:
CIR	rB_7:
CIL	rB_6:
INC	rB_5:
SPA	rB_4:
SNA	rB_3:
SZA	rB_2:
SZE	rB_1:
HLT	rB_0:

5. (a) Draw and explain the Input-Output interface with Accumulator.
(b) Write all the Input-Output Instructions with RTL for: