JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT
TEST -2 EXAMINATION-2022
M.Tech-I Semester (ECE)

COURSE CODE (CREDITS): 21M11EC112 (3) MAX. MARKS: 25
COURSE NAME: Embedded Systems and Applications
COURSE INSTRUCTORS: Er. Munish Sood MAX. TIME: 1 Hour 30 Min

Note: *All questions are compulsory. Marks are indicated against each question in square brackets.*

Q1. Explain in detail about ARM architecture. What are the features used and rejected from RISC design? **(3) CO2**

Q2) What are the different ARM registers? Explain in detail about current program status register (CPSR)? How are exceptions handled in ARM? **(3) CO3**

Q3) Explain the different operating modes in ARM? What is the load store architecture used in ARM? What are a 'hit' and a 'miss' in ARM? How do we calculate the 'hit rate' and 'miss rate'? **(3)CO3**

Q4) What are the different types of assembly language programming used in ARM? Give examples of different data processing instructions used in ARM. **(3) CO3**

Q5) With the help of a block diagram explain the architecture of a PIC microcontroller. **(3) CO3**

Q6) Give the results of the instructions executed in ARM **(5) CO2**

(i) ADC r_0, r_1, r_2
(ii) SBC r_0, r_1, r_2
(iii) ORR r_0, r_1, r_2
(iv) MOV r_0, r_2
(v) MLA r_4, r_3, r_2, r_1

Q7) Give the results of the instructions executed in a PIC microcontroller (given in bold) the contents of work register W and other memory locations are specified in each case. **(5) CO2**

(i) Before instruction `W=0X55;` **`CLRW`**
(ii) Before instruction `REG=0XF3;` **`SWAP REG,0`**
(iii) Before instruction `FSR=0XC2,` and `W=0X00;` **`MOVF FSR,0`**
(iv) Before instruction `W=0X17,FSR=0XC2;` **`ADDWF FSR,0`**
(v) Before instruction `W=0X17,FSR=0XC2;` **`ANDWF FSR,1`**