Neeru Sharma

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -2 EXAMINATION- Oct 2019

B.Tech VIIth Semester(CSE/IT)

COURSE CODE: 12B1WEC732 MAX. MARKS: 25

COURSE NAME: Digital System Design

COURSE CREDITS: 3 MAX. TIME: 1.5Hrs

Note: *All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means.*

---

1 Reduce the following state table using a merger diagram and compatibility graph **[5]**

Present State	Next State/Output	
	0	1
a	b/1	h/1
b	a/0	g/0
c	-/0	f/-
d	d/0	-/1
e	c/0	d/-
f	a/-	c/0
g	-/-	b/-
h	g/0	e/-

2 For the given state table, apply the state assignment techniques and justify your **[5]**

Present State	Next State, X	
	0	1
A	A	C
B	C	D
C	A	F
D	B	E
E	C	C
F	D	E

3 Reduce the following incompletely specified state table using implication chart. Also identify the compatible pairs **[5]**

Present State	Next State		Output	
	x= 0	x= 1	x= 0	x= 1
a	a	b	0	-
b	c	b	0	1
c	d	a	-	1
d	a	c	0	-
e	e	a	-	0

4 **(a)** Explain the building block of ASM charts in detail **[3]**

(b) Design a sequence detector that will detect the following sequence 1011. Overlapping is permitted. **[2]**

5 **(a)** What is maximum compatibility? What is the difference between compatible states and maximal compatibility? **[3]**

(b) Describe in your own words the difference between fundamental and pulse mode asynchronous sequential circuits. **[2]**