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JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -2 EXAMINATION- October 2019

B.Tech III Semester (ECE)

COURSE CODE: **18B11EC312** MAX. MARKS: 25

COURSE NAME: **DIGITAL ELECTRONICS AND LOGIC DESIGN**

COURSE CREDITS: 04 MAX. TIME: 1Hr 30 min

***Note:** All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means.*

1. For given function $f(A, B, C, D) = \sum m(2, 3, 4, 5, 7, 8, 10, 13, 15)$ find the following.
   a) Realize the minimized expression using NOR gate
   b) Implement the function using 4:16 decoder **[2.5 + 2.5 = 5] [CO3]**
2. Use Karnaugh maps to find the minimum-cost SOP and POS expressions for the function $f(x_1, x_2, x_3, x_4) = \overline{x_1}\,\overline{x_3}\,\overline{x_4} + x_3 x_4 + \overline{x_1}\,\overline{x_2} x_4 + x_1 x_2 \overline{x_3} x_4$ assuming that there are also don't-cares defined as $d = (8, 9, 12, 13)$. **[2.5 + 2.5 = 5] [CO3]**
3. In a certain application, four inputs A, B, C, D (both true and complement forms available) are fed to logic circuit producing an output F, which operates a relay. The relay turns ON when f (A, B, C, D) = 1 for the following stats of inputs (ABCD) : 0000, 0010, 0101, 0110, 1101, and 1110. States 1000 and 1001 do not occur and for the remaining states the relay is OFF. Implement the logic function using 4:1 multiplexer. **[5] [CO3, CO4]**
4. a) Design a parity generator to generate even parity bit for a 3 bit word using 1:8 demultiplexer. Which other combinational circuit gives the same output.
   b) Design a combinational circuit to perform the operation: 587 - 425 .
   c) Implement 4 bit prime number detector using AOI logic. **[2 + 1.5 + 1.5 = 5] [CO4]**
5. a) Give the Boolean expression of F shown in fig 1 implemented by the given CMOS logic
   b) Assuming each transistor as an ideal switch, specify the states (ON state or OFF State) of each transistor when A = C = Logic 1, while B = D = Logic 0.
   c) Explain the four regions in which BJT works by specifying input and output.
   d) Draw a diagram of Diode Transistor Logic.

[1+ 1 + 1 + 2 = 5] [CO1, CO2]

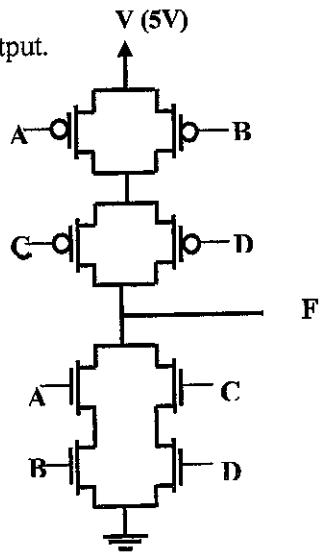

Fig 1