JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -2 EXAMINATIONS-2022

B.Tech-V Semester (CS/IT)

COURSE CODE (CREDITS): 18B11CI514 (3) MAX. MARKS: 25

COURSE NAME: Computer Organization & Architecture

COURSE INSTRUCTORS: Dr. Vivek, Dr. Pardeep, Sh. Praveen, Dr. Pankaj & Dr. Vipul

MAX. TIME: 1 Hour and 30 Minutes

Note: All questions are compulsory. Marks are indicated against each question in square brackets.

Q1. **a.** Consider a 4-way set associative mapping with **16** cache blocks. The memory block requests are in the order- **{0, 255, 1, 4, 3, 8, 133, 159, 216, 129, 63, 8, 48, 32, 73, 92, 155}**. If **LRU** cache replacement policy is used, which cache block will not be present in the cache? Also, calculate the hit ratio and miss ratio. [3] CO[3]

b. A disk pack has **25** surfaces, storage area on each surface has an inner diameter of **50 cm** and an outer diameter of **30 cm**. The minimum storage density on any track is **4000 bits/cm**, minimum spacing between the tracks is **0.5 mm** and width of the track is **0.2 mm**. Compute the capacity of the disk pack along with data transfer rate, if disk is rotating at **5000 RPM** using two R/W heads. [3] CO[3]

Q2. **a.** Given an **8** bit data string: **00111001**. Compute the parity bits for the given data string. Now let us assume that the **third bit** is corrupted. Use Hamming code to detect and correct the corrupted bit. [3] CO[4]

b. The width of the physical address on a machine is **40** bits. Compute the width of the tag field in a **512** KB **8**-way set associative cache. [3] CO[3]

Q3. **a.** In a two level virtual memory, the memory access time for main memory is **10^-8** seconds and the memory access time for the secondary memory is **10^-3** seconds. What must be the hit ratio, such that the access efficiency is within **80%** of its maximum value? [3] CO[4]

b. What is the difference between static RAM & dynamic RAM? [3] CO[4]

[P.T.O]

Q4. **a.** The memory access time is **1** nanosecond for a read operation with a hit in cache, **5** nanoseconds for a read operation with a miss in cache, **2** nanoseconds for a write operation with a hit in cache and **10** nanoseconds for a write operation with a miss in cache. Execution of a sequence of instructions involves **100** instruction fetch operations, **60** memory operand read operations and **40** memory operand write operations. The cache hit-ratio is **0.9**. Compute the average memory access time (in nanoseconds) for executing the sequence of instructions. [3] CO[3]

b. Find out the minimum number of drives you will need to implement RAID 0, RAID 1, RAID 10, RAID 2, RAID 3 and RAID 6. [3] CO[4]

Q5. How many multiplexers, comparators, OR gates and AND gates are needed to implement an associative cache comprising of **8** cache lines? [1] CO[3]