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TEST -3 EXAMINATION- May 2019

B.Tech VI Semester

COURSE CODE: 10B11EC612 MAX. MARKS: 35

COURSE NAME: VLSI TECHNOLOGY AND APPLICATIONS

COURSE CREDITS: 04 MAX. TIME: 2 Hrs

***Note:** All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means.*

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1. **[CO1, CO2, CO3, CO4, CO5][1 * 10 =10]**

I. _____(nMOS/ pMOS) can pass a logic 0 perfectly, but cannot pass a logic 1 perfectly.

II. AND terms are realized by _____connections of nMOS in pull down network.

III. Two input NOR gate requires six transistors in CMOS logic _____(True / False)

IV. In full scaling, the power dissipation is _____ (decreased by a factor S^2/ increased by S^2)

V. Assuming depletion load, draw the logic diagram for $\overline{A(B+CD)}$.

VI. Does the substrate bias affect CMOS circuits? How.

VII. Specify the notation for *p*-diffusion, and *n*- substrate used for fabrication process.

VIII. Express the formulas for small signal parameters?

IX. In pass transistors for n-MOS, if $V_i > V_{max}$ than what is the output of the transistor? Assume gate voltage as V_{DDG}, source voltage as V_{DD} and threshold voltage as V_{thn}.

X. For _____ (NAND/ NOR) gate the effective length of the driver transistors doubles.

2. A CMOS NOR2 gate is designed using *n*-MOS with a value of k_n. The *p*-MOS are both described by $k_p = 2.2\ k_n$. Find the value of midpoint voltage for the case of simultaneous switching if the power supply is 3.3V, threshold voltage for *n*-MOS is 0.65V and threshold voltage for *p*-MOS is -0.80V. **[CO1, CO4] [5]**

3. Consider a CMOS inverter circuit with the following parameters : $V_{DD} = 3.3V$, $V_{TO,n} = 0.6V$, $V_{TO,p} = -0.7V$, $k_R = 2.5$. Calculate Low noise margin **[CO4] [5]**

4. In the inverter circuit what is meant by Z_{pu} / Z_{pd}? Derive the required ratio between Z_{pu} / Z_{pd} if an *n*MOS inverter is to be driven from another *n*MOS inverter. Assume $V_{th} = 0.3V_{DD}$, and $V_{thdep} = -0.7V_{DD}$ **[CO6] [5]**

5. Explain the different steps of fabrication for enhancement *n*-type MOSFET **[CO5] [5]**

6. Draw the stick diagram of the logic expression $f(A,B,C) = \overline{A+B(C+D)}$ using CMOS logic. Find the equivalent circuit for *n*MOS transistor only, assuming that $(W/L)_n = 10$ for all *n*-MOS transistor. **[CO5] [5]**