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JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT
TEST-2 EXAMINATION- APRIL -2019
B.Tech VI Semester

COURSE CODE: 10B11EC612 MAX. MARKS: 25
COURSE NAME: VLSI TECHNOLOGY AND APPLICATIONS
COURSE CREDITS: 04 MAX. TIME: 1 HRS 30 MIN

Note: *All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means.*

1. **(CO1, CO4) [1 × 5 = 5]**

(a) How Logic Swing is different from Transition width?

(b) An *n*MOS is turned ON if its gate is connected to _____voltage. On the other hand, a *p*MOS is turned ON if its gate is connected to _____voltage.

(c) Calculate the noise margin of a digital logic circuit having the following information: V_{IL} = 0.6V, V_{IH} = 1.5V, V_{OL} = 0.2V and V_{OH} = 1.8V.

(d) The value of oxide related capacitance C_{GB} is C_{ox} *W L* in cutoff region. Explain.

(e) What is gate drain overlap? What is its effect? Show gate drain overlap in MOS structure.

2. Consider *n*- channel enhancement MOSFET having following physical parameters: grading coefficient for junction, 0.26; the grading coefficient for sidewall, 0.1; width, 5μm; length of drain, 3μm; length of channel, 0.5 μm; built in voltage, 0.7V; built in voltage for sidewall, 0.9V; C_{sb0} = 0.86 fF/μm^2 , C_{db0} = 0.24 fF/μm^2 , C_{sbsw} = 0.24 fF/μm , C_{dbsw} = 0.24 fF/μm, abrupt junction depth, 0.4μm; reverse bias voltage 3V. Find source substrate diffusion capacitance. **(CO3) [6]**

3. An *n*-MOS transistor is fabricated with the following physical parameters: $N_{D(poly)} = 10^{20}cm^{-3}$, $N_{A(substrate)} = 10^{16}cm^{-3}$, *W* = 10μm, *Y* = 5μm, *L*= 1.5μm, V_{DB} = 2V to 4V, gate to source voltage = 4V, drain to source voltage = 4V. Find drain capacitance for the MOSFET assuming parasitic capacitance as junction. **(CO1, CO3) [6]**

4. **(CO4) [2 × 4 = 8]**

(*a*) Calculate the critical voltages of a resistive load *n*-MOS inverter, using the following information: V_{DD} = 5.0 V, k_n = 50μA/V^2, V_{t0D}= 0.5V, R = 100KΩ.

(*b*) Determine the V_{OH} and V_{OL} for Linear E-MOS inverter when biased at V_{GG} = 4V, V_{DD} = 3V, *k*'=100μA/V^2, V_{t0D} = 1V, V_{t0L}= 0.8V, $(W/L)_D$ =40/4 and $(W/L)_L$= 28/2.