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TEST-1 EXAMINATION- FEBRUARY -2019

B.Tech VI Semester (ECE)

COURSE CODE: 10B11EC612 MAX. MARKS: 15
COURSE NAME: VLSI TECHNOLOGY AND APPLICATIONS
COURSE CREDITS: 04 MAX. TIME: 1 HRS

Note: *All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means.*

1.

(a) What is the role of architectural specification, timing and relationship between functional units and layout in the VLSI design cycle?

(b) Explain the accumulation, depletion and inverse region when MOS system works under external bias for an *n*-channel MOS transistor. **[2 + 3 = 5]**

2.

Consider following parameters for Depletion *n*-channel MOSFET : gate oxide thickness = 345Å, aspect ratio= 1.0, electron mobility= 500 cm^2/ V.sec, $|2\phi_f| = 0.84V$.

Some laboratory measurements results of terminal behavior of this device are shown in table 1. Using the data in the table, find the missing value of the gate voltage in the last entry. Show all of the details of your calculation.

I_{DS} (μA)	V_D	V_S	V_B	V_G
50	3V	0	0	0
40	5V	3V	0	?

[5]

3. Derive the following equations where each symbol has its typical meaning

a) $g_m = \sqrt{2 i_D k}$

b) $r_o = \left[\lambda\left(k'/2\right)\left(W/L\right)\left(V_{gs} - V_{th}\right)^2\right]^{-1}$

c) $i_D = \frac{k}{2}\left(V_{gs} - V_{th}\right)^2\left(1 + \lambda V_{ds}\right)$ (Note : show only the channel length modulation)

[1 + 2 + 2 = 5]