Dr. Kapil Sharma.

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT
TEST -1 EXAMINATION- February-2020
VIII Semester

COURSE CODE: 18B1WCI837 MAX. MARKS:15
COURSE NAME: Advance Computer Architecture
COURSE CREDITS: 03 MAX. TIME: One Hours

Note: *All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means.*

1. Choose the correct option [1+1+1]

A. Which of the following statement is false with respect to instruction pipeline
   a) Pipeline can increase the throughput of system
   b) Pipeline partition the system into multiple independent stages with added buffers between the stages
   c) Pipeline reduce the latency of each individual instruction
   d) Unbalance latency of pipeline stages reduces overall speed

B. Which of the following can be a valid instruction for an Accumulator architecture (Note: A is address of memory location and R is the name of Register)
   a) Load A b) Push A c) Load R, A d) Add R, A

C. Which one is not a hazard in instruction pipeline
   a) Structural b) Data c) Control d) Operand forwarding

2. Assume an expression A = D * (B + C) – E is executed on Register-Resister/ Load-Store architecture. Write the sequence of instruction for executing this expression on given architecture? [3]

3. A new multimedia unit (MU) is added in a processor speed up the completion of multimedia instruction given to the processor by 4 times. Assuming a program has 40% multimedia instructions, what is the overall speed up gained while running the program when it is executed on the processor with new MU than when it is run on the processor without this MU. [3]

4. Consider two programs A and B that solve a matrix inversion problem. A is schedule to run on a processor P1 operating at 1.1 GHz and B is schedule to run on processor P2 operating at 1.25 GHz. Program A have total 7500 instructions, out of which 15% are branch instructions, 47% are load store and remaining are ALU instructions. Program B have total 6200 instructions, out of which 35 % are branch instructions, 23% are load store and remaining are ALU instructions. In processor P1 load store instruction has an average clock per instruction (ACPI) 7 cycle, branch instruction have ACPI 3 and ALU instruction have ACPI 4 cycles. Similarly at processor P2 load store instruction has an average clock per instruction (ACPI) 4 cycle, branch instruction have ACPI 5 and ALU instruction have ACPI 3 cycles. Find which mapping solves matrix inversion problem faster? [3]

5. Assume a seven stage pipeline system, with zero latch duration, execute the program contains 35 instructions. Also assume there is no hazard in these instructions for preventing parallel execution. If each stage takes one CPU cycle to complete one instruction, find the number of CPU cycles to compute the program. [3]