Analytical Model for Optimum Signal Integrity in PCB Interconnects Using Ground Tracks

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***Abstract*—In this paper, we present analytical models for line impedance and the coupling coefficient in the presence of additional ground tracks. We use a variational analysis combined with the transverse transmission-line technique to model interconnect lines guarded by ground tracks. Using the proposed model, it would be possible for designers to reduce crosstalk in coupled lines and obtain desired line impedance, thereby ensuring optimum signal integrity. The results obtained are verified by full-wave simulations and measurements performed on a vector network analyzer. The proposed model may find applications in the design and analysis of high-speed interconnects.**

***Index Terms*—Crosstalk, finite-difference time-domain (FDTD), ground tracks, printed circuit board (PCB) interconnects, signal integrity, variational analysis.**

I. Introduction

COUPLED noise between interconnect lines is a potential cause of failure in high-speed digital systems [1]–[3]. Grounded printed circuit board (PCB) tracks are often used for reduction in crosstalk in a variety of routing topologies and mixed-signal systems [4]–[7]. High-speed interconnects are essentially microstrip transmission lines with their characteristic impedance being related to the width of the strip, the height of the substrate, and the dielectric constant of the substrate [8]. However, with the introduction of an additional ground plane adjacent to the signal strip, the line properties can change significantly. The line impedance now becomes a function of the separation between the interconnect line and the ground tracks.

Various analytical methods have been reported for computing the impedance of a microstrip line and for evaluating crosstalk in coupled microstrip lines. These include the conformal transformation method [9], the variational method [9]–[11], the finite-difference method [12], and the boundary element method [13]. These techniques are applied to compute the characteristic impedance of a variety of microstrip-like interconnects [14]–[23]. In case of coupled lines, it is imperative for a designer to verify if a given routing topology will lead to logic failures due to coupled noise. Such verification is typically done using capacitive charge sharing models or exhaustive simulations. The simulation models are pessimistic and time-consuming [24]–[30], so there is a need for simpler methods with better accuracy. Although the use of ground tracks is by far the best remedy for crosstalk-related problems, signal integrity could only be achieved using a more elaborate design model that uses ground tracks not only for crosstalk attenuation but also for achieving desired line impedance.

In this paper, we propose closed-form expressions for the characteristic impedance of an interconnect line flanked by ground tracks on either side and for coupling coefficients in coupled interconnects separated by an intermediate ground track acting as a shield line. The proposed results are verified by finite-difference time-domain (FDTD) simulations and measurements performed on a vector network analyzer, which exhibits high accuracy. Using our model, it would be possible for designers to strategically place ground tracks so as to achieve desired line impedance along with crosstalk mitigation, thus ensuring overall signal integrity. The analytical model has been developed using a variational method combined with the transverse transmission-line technique [3].

Out of all the analytical methods mentioned before, the variational method treats the dielectric boundary conditions in a generalized way. Thus, it is also possible to analyze multilayer microstrip lines without much difficulty. The accuracy of this method is insensitive to the choice of the trial function [3]. The method is based on the calculation of the line capacitance by the static field theory, and therefore is an approximation to the electromagnetic (EM) theory. The conformal mapping technique may become prohibitively complicated in the case of inhomogeneous transmission-line structures. Also, the finite-difference method involves a numerical evaluation and is thus limited to simpler structures. On the other hand, the variational method—although approximate-–offers a simpler way of determining propagation parameters of microstrip-like interconnects. When combined with the transverse transmission-line techniques of determining the Green's function [23], the derivation for the capacitance of the interconnect line becomes quite simple and has reasonable accuracy with lesser computation time. All of this makes the variational method combined with the transverse transmission-line technique a natural choice for the analysis of the interconnect structures in our paper.

While crosstalk reduction using additional ground tracks has been discussed in detail [7], the effect of such ground tracks on the impedance of the interconnect line itself is usually neglected. From the point of view of system design, one has to look into these issues in conjunction, if signal integrity is to be safeguarded. This happens to be the motivation behind our

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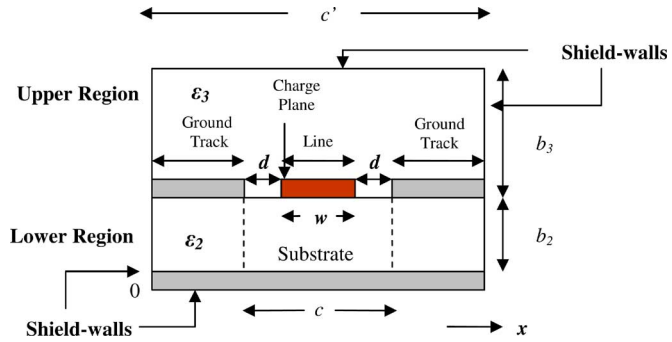


Fig. 1. Lateral view of the interconnect structure guarded by ground tracks.

present research. We report systematic design steps whereby ground tracks can be intelligently placed to ensure desired line impedance and crosstalk attenuation, thus guarantying optimum signal integrity and is valid up to reasonable range of frequencies. In our view, the proposed model may be useful to practicing signal integrity engineers and designers and can be applied to PC board and RF interconnects modeling. To the best of the authors' knowledge, no such model has been previously reported that tackles both these problems in conjunction. The novelty of our research lies in the computation admittance parameters for single as well as coupled interconnects lines flanked by adjacent ground lines. The placement of ground tracks adjacent to the signal interconnects imposes modified boundary conditions that require recalculation of the admittance parameters.

The following sections present the proposed model and the analytical results compared with simulated and measured data. Illustrations are provided to show the how signal integrity can be improved in specific interconnect structures using this model.

II. Analytical Model for Line Impedance

A. Proposed Model

Fig. 1 shows the cross section of the interconnect line that is at the center over a ground plane at the bottom and resembles a standard microstrip-like structure. In order that the interconnect line carrying a signal is isolated, grounded metallic traces have been placed on both sides of the line. The interconnect line is assumed to be very thin having a width "w." The thickness of the dielectric (lower region) is b_2 having a permittivity ε_2. The ground tracks, coplanar with the interconnect line, have a separation "d" from the line on both sides. Therefore, the interconnect line sees grounded planes both below vertically and sideways laterally.

The standard technique for determining line capacitance is explained in detail in [3], and hence, only salient steps leading to the variational formula for the capacitance are presented here. The variational expression for the capacitance of a multilayer structure, as shown in Fig. 1, is given by

$$C = \frac{(1+0.25A)^2}{\sum_n \left((L_n + AM_n)^2 P_n / Y\right)} \tag{1}$$

where

$$\begin{aligned}
L_n &= \sin(\beta_n w/2);\\
M_n &= (2/\beta_n w)^3 [3\left\{(\beta_n w/2)^2 - 2\right\}\cos(\beta_n w/2)\\
&\quad + (\beta_n w/2)\left\{(\beta_n w/2)^2 - 6\right\}\sin(\beta_n w/2) + 6];\\
P_n &= (2/n\pi)(2/\beta_n w)^2;\\
\beta_n &= n\pi/c;\\
A &= -\frac{\sum_{n\text{odd}} (L_n - 4M_n)\, L_n P_n / Y}{\sum_{n\text{odd}} (L_n - 4M_n)\, M_n P_n / Y};\\
n &= 1,\ 2,\ 3, \ldots, \infty.
\end{aligned}$$

In order to apply (1) to the interconnect structure under study, it is first necessary to determine the boundary conditions that are given as electric wall and/or magnetic wall. Thus, explicit expressions can be established for the Green's function $G(x, x_0/y_0, y_0)$ for three separate cases.

1) Electric walls at $x = 0$ and c.
2) Electric wall at $x = 0$ and magnetic wall at $x = c$.
3) Magnetic walls at $x = 0$ and c.

It may be of interest to the reader that using the transverse transmission-line technique, the problem of determining Green's function reduces to that of determining the admittance at the charge plane $y = y_0$. Note that in (1), the only parameter that needs to be determined is the admittance Y at the charge plane $y = y_0$. To compute the admittance Y, we take shield walls (both lateral and top) in the upper and lower regions. The expression for the admittance is easily obtained by applying standard transmission-line formula for the input admittance $Y_{\text{in},j}$ of a section of the transmission line with characteristic impedance $Y_{cj} = \varepsilon_j = \varepsilon_0 \varepsilon_{rj}$, propagation constant γ_j, and length l_j. For sake of completion, the method of computing the admittance is outlined as next.

Fig. 1 is a two-layer structure with the bottom layer given by dielectric 1 (ε_2, b_2) and the top layer given by dielectric 2 (ε_3, b_3) bounded by electric shorts on all four sides. We are interested to compute the admittance at the interface of layers 1 and 2, which is the charge plane. For such computation, we use the standard transmission-line formulation

$$Y_{\text{in},j} = \varepsilon_j \left[\frac{Y_{ij} + Y_{cj}\tanh(\gamma_j l_j)}{Y_{cj} + Y_{ij}\tanh(\gamma_j l_j)}\right].$$

If we now consider the admittance (Y_{-}) seen at the charge plane due to layer 1, we obtain the result as

$$\begin{aligned}
Y_{\text{Lower},n} &= \varepsilon_0 \varepsilon_2 \coth(\beta_n b_2)\\
\beta_n &= \frac{n\pi}{c}\\
c &= 2d + w.
\end{aligned} \tag{2}$$

This is obtained since $Y_{ij} = \infty$ (electric short at the bottom). In this case, ε_2 and b_2 are the permittivity and the height of the dielectric layer, respectively, and the capacitance is computed for odd values of n excluding $n = 0$. The distance c is shown

by dotted lines. Similarly, $Y_{\text{in},j}$ is iterated over each section of the transmission line to determine the individual admittances of the lower and upper regions and summing them to obtain Y at the charge plane. The admittance of the upper region is given by

$$\begin{aligned} Y_{\text{Upper},n} &= \varepsilon_0 \varepsilon_3 \coth(\beta_n b_3) \\ \beta_n &= \frac{n\pi}{c'} \\ c' &\gg w \\ b_3 &\gg b_2 \end{aligned} \tag{3}$$

where ε_3 and b_3 are the permittivity and the height of the dielectric layer (upper region), respectively, and is computed for even values of n excluding $n = 0$. Here, c' is a variable distance and is kept much greater than the line width "w." Substituting (2) and (3) in (1), we compute the line capacitance for these two regions, C_{Lower} and C_{Upper}, respectively. The total capacitance will now be the summation of C_{Lower} and C_{Upper}. With increasing value of sidewall spacing, the effect of sidewalls on the capacitance of the structure reduces, and for a sufficiently large value, the capacitance approaches that of the structure with no sidewalls. The same method is applied in [31] to different structures by combining the admittance for both lower and upper regions. However in the present case, individual admittance parameters are used to evaluate the capacitances for both lower and upper regions, and the resultant capacitance is obtained by summing these two. This difference is introduced to obtain an equivalent representation of the practical microstrip layout. As shown in Fig. 1, the separation "c" of the lateral shield walls is a parameter that can be used to tune the characteristic impedance and the coupling between the lines. However, for an open microstrip line, the upper layer has no lateral or top shield walls. This can be analyzed by considering c' and b_3 to be large values as compared to "w" the width of the line.

It can be seen that as the separation "d" increases, the admittance parameter Y_{Lower} modifies and the formulation given before reduces to that of a basic microstrip line. The results are valid for a range of dielectric substances and can be equally used for multilayer structures. It may be of interest to readers that the proposed analysis is quasi-static in nature, and is thus valid for low-frequency applications. However, the results obtained in this paper are accurate up to 5–7 GHz (for electrically thin substrates), which happens to be the frequency of interest in current high-speed interconnects.

The capacitance formula given by (1) is applicable to any single conductor stripline-like transmission-line interconnects with one or more dielectric layers. If the interconnect has a small but finite thickness "t," (1) can still be used by replacing Y in (2) and (3) by $Y/h\,(\beta_n, t)$, as reported in [3]. The expression $h\,(\beta_n, t)$ for the structure considered is given by

$$h(\beta_n,\ t) = \frac{1}{2}\left[1 + \frac{\sinh\{\beta_n\,(b_2 - t)\}}{\sinh\{\beta_n b_2\}}\right]. \tag{4}$$

From the expression for the characteristic impedance of a microstrip line [11], the impedance Z of the interconnect structure is

$$Z = \frac{1}{v^a\sqrt{(C_{\text{Lower}} + C_{\text{Upper}})(C^a_{\text{Lower}} + C^a_{\text{Upper}})}}. \tag{5}$$

Here, superscript "a" denotes free space dielectric. The previous set of equations gives a simple design methodology that aids in fast and efficient computation of the characteristic impedance Z of the proposed interconnect structure.

B. Results

We have used accurate commercial software CST Microwave Studio for obtaining simulation results. Fig. 2 gives a comparative plot of the characteristic impedance of an interconnect line with adjacent grounded guard tracks for a range of dielectric substrates ($\varepsilon_r = 2.2$, 4.6, and 9.9). It is interesting to note that the characteristic impedance Z reduces substantially when the ground tracks are placed close to the interconnect lines. The introduction of guard tracks close to the interconnect line results in an increase in the lateral capacitance between the line and the guard tracks, thus reducing the characteristic impedance of the interconnect line, as shown in Fig. 3.

The results are validated by measurements performed on fabricated interconnect structures of different specifications using a vector network analyzer. The measurements were performed at $f = 1.5$ GHz, and the measured results are highlighted in Fig. 2. The theoretical results show good agreement with the measured data, which validates our analysis. As a special case, when the distance between the line and the ground tracks increases, the characteristic impedance Z approaches a final value, which corresponds to that of a microstrip line, as shown in Table I. The results obtained using our analysis show good agreement with available data [8] and prove that the aforementioned analysis can also be practically used for the analysis of microstrip lines.

C. Characteristic Impedance Versus Frequency

As stated before, the proposed model is quasi-static, and hence limited for higher frequency applications. It is seen that the proposed model gives fairly accurate results up to 5–7 GHz. This is clearly illustrated in Fig. 4. The simulated results are obtained up to 10 GHz and compared with the analytical results. The analytical results being independent of frequency are shown as straight lines. However, in case of microstrip-like lines, dispersion phenomenon is witnessed at higher frequencies. The dispersive effects are due to open microstrip conditions and the frequency dependence of the loss tangent and effective dielectric constant. Also, it can be seen that dispersion is more dominant in materials with higher dielectric constants and height. However, in most of the cases, our results corroborate with the simulated data up to 5–7 GHz as mentioned earlier. From the aforementioned results, one can derive the extent of error in actual impedance compared with the analytical results. This is tabulated in Table II. The percentage error is given at 7 GHz.

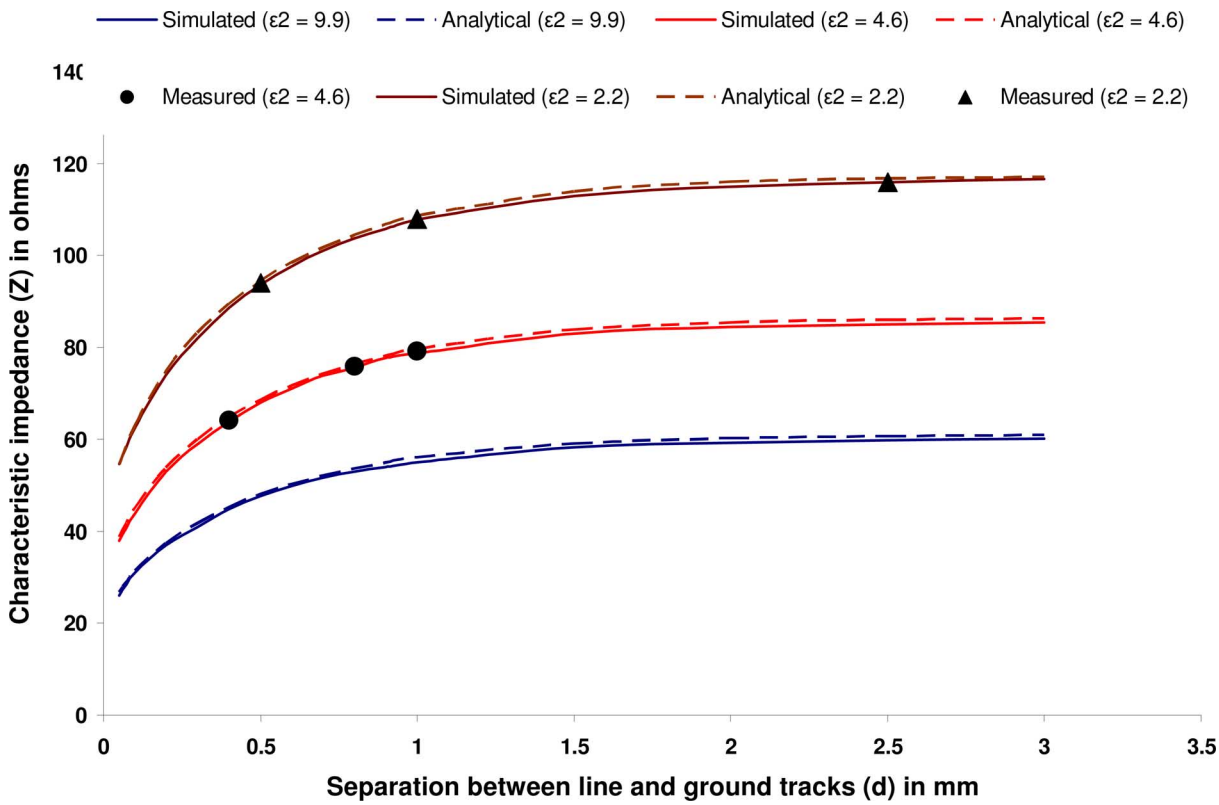


Fig. 2. Simulated, predicted, and measured characteristic impedance ($w = 1$ mm and $h = 1.59$ mm).

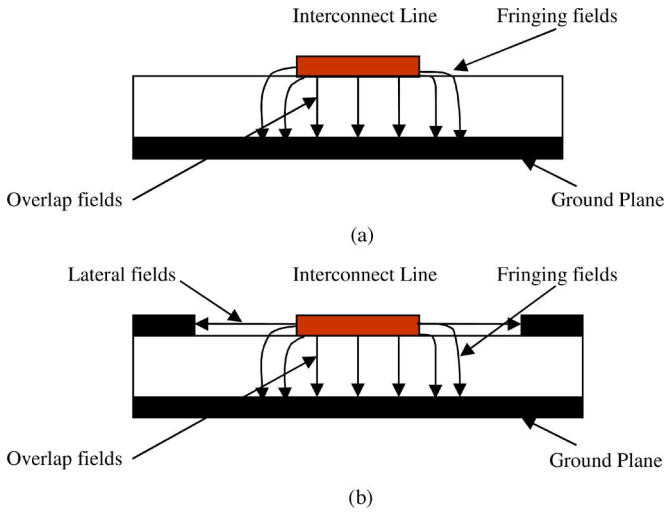


Fig. 3. (a) Field distribution in the interconnect structure (without ground tracks). (b) Field distribution in the interconnect structure (with ground track).

TABLE I
CHARACTERISTIC IMPEDANCE z FOR A MICROSTRIP LINE

w/b₂	*Theoretical results*	*Wheeler's formula [8]*
0.8	85.59 Ω	83.74 Ω
1.6	60.91 Ω	59.21 Ω
2.4	47.53 Ω	46.39 Ω

$\varepsilon_r = 3.78$ and $d = 5$ mm.

III. ANALYTICAL MODEL FOR CROSSTALK

A. Proposed Model

We now present the analysis of coupled lines separated by an intermediate ground track, using the variational method, for the estimation of crosstalk. Fig. 5 shows the lateral view of a multilayered edge-coupled transmission structure with a rectangular shield enclosure.

The variational expression for the capacitance is given by

$$C_{\text{odd}}^{\text{even}} = \frac{(1 + 0.25A_{\text{odd}}^{\text{even}})^2}{\sum_{n_{\text{even}}^{\text{odd}}} (L_n + M_n A_{\text{odd}}^{\text{even}})^2 P_n / Y} \tag{6}$$

$$L_n = \sin(\beta_n w/2) \sin\left\{\beta_n \left(\frac{c-s-w}{2}\right)\right\};$$

$$M_n = (2/\beta_n w)^3 \sin\left\{\beta_n \left(\frac{c-s-w}{2}\right)\right\} \times \begin{bmatrix} 3\left\{(\beta_n w/2)^2 - 2\right\}\cos(\beta_n w/2) \\ +(\beta_n w/2)\left\{(\beta_n w/2)^2 - 6\right\}\sin(\beta_n w/2) + 6 \end{bmatrix};$$

$$P_n = (4/n\pi)(2/\beta_n w)^2$$

$$\beta_n = n\pi/c$$

$$A_{\text{odd}}^{\text{even}} = -\frac{\sum_{n_{\text{even}}^{\text{odd}}} (L_n - 4M_n) L_n P_n / Y}{\sum_{n_{\text{even}}^{\text{odd}}} (L_n - 4M_n) M_n P_n / Y}.$$

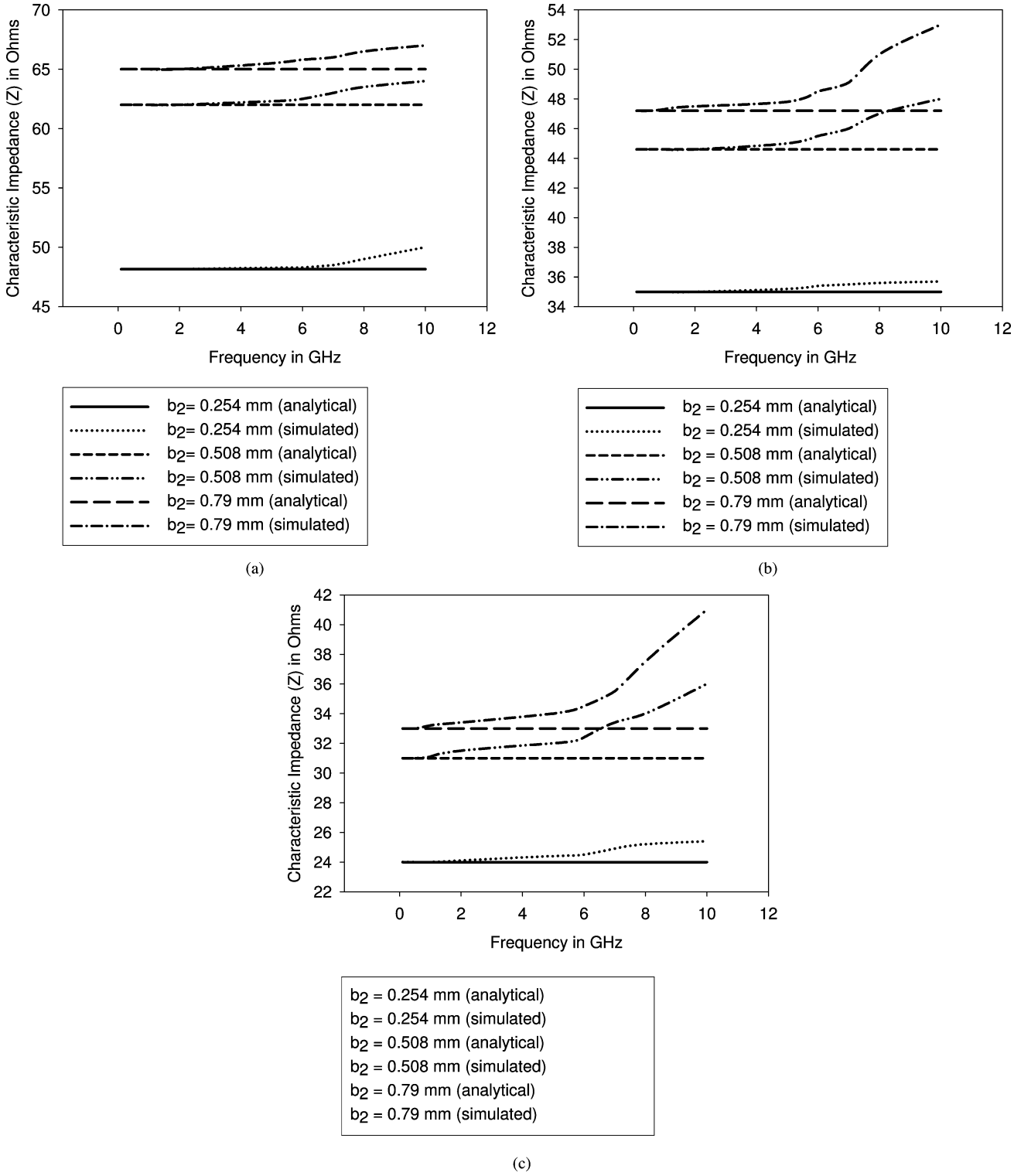


Fig. 4. (a) Simulated and analytical characteristic impedance ($w = 0.78$ mm, $\varepsilon_2 = 2.2$, $d = 0.1$ mm). (b) Simulated and analytical characteristic impedance ($w = 0.78$ mm, $\varepsilon_2 = 4.6$, $d = 0.1$ mm). (c) Simulated and analytical characteristic impedance ($w = 0.78$ mm, $\varepsilon_2 = 9.9$, $d = 0.1$ mm).

The capacitance formula is derived in detail in [3]. The only parameter that needs to be computed in the previous formula is the admittance Y of the structure at the charge plane $y = y_0$. The placement of a ground track between the two signal-carrying conductors alters the method of computing the admittance on the charge plane from that for conventional microstrip line coupler. This can be explained by observing the field lines for the two modes, namely odd and even modes.

Fig. 6 shows the electric field lines for the two modes necessary for computation of the coupling factor. From Fig. 6, it is

TABLE II
PERCENTAGE ERRORS BETWEEN THE ANALYTICAL AND SIMULATED CHARACTERISTIC IMPEDANCE

ε_2	b_2	% Error
2.2	0.254 mm	0.7
	0.508 mm	1.41
	0.79 mm	1.53
4.6	0.254 mm	1.42
	0.508 mm	3.13
	0.79 mm	4.01
9.9	0.254 mm	3.75
	0.508 mm	4.51
	0.79 mm	7.01

$w = 0.76$ mm, $d = 0.1$ mm, and $f = 7$ GHz.

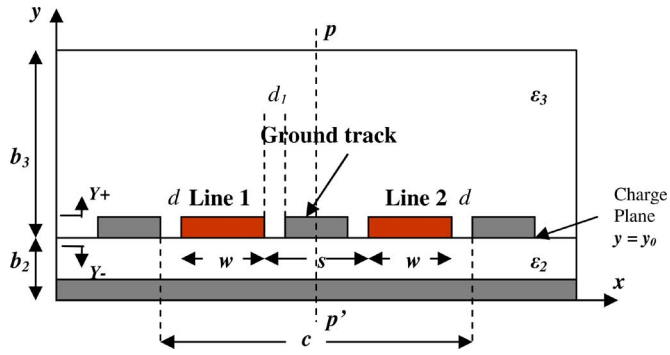


Fig. 5. Edge-coupled transmission-line structure with intermediate ground track.

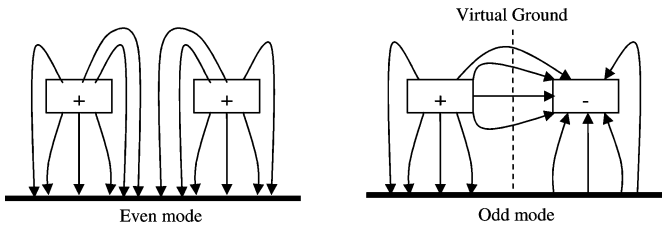


Fig. 6. Even- and odd-mode electric field lines.

evident that the odd-mode capacitance is computed by considering an electric wall (virtual ground) between the two conductors. Therefore, a physical placement of a ground between the two conductors does not in any way alter the computational method. However, for the computation of the even-mode capacitance, we generally consider a magnetic wall between the two conductors. In the present case, however, there exists a physical placement of an electric wall between the two conductors. This ground track extends from the ground plane below the substrate to the charge plane only. Therefore, the admittance presented by the lines now depends on the lateral dimension of wall-to-wall spacing, which, in this case, is given by

$$g = 2(d + w + d_1)$$

where "d_1" is the separation of the line to inner ground track taken edge to edge. Since for the even mode both the signal-carrying lines are at same potential, the electric fields also get terminated at the lateral ground as well as the ground plane below. Now the boundary condition used for computation with respect to the plane of symmetry pp' (refer to Fig. 5) changes to an electric wall at $x = 0$ and an electric wall at $x = g/2$. For such a computation of the even-mode capacitance, we need to only consider the line-to-line separation as $s = 2d_1$.

1) Computation of Odd-Mode Impedance: For computing odd-mode impedances, we assume electric boundaries at $x = 0$ and $x = c/2$. The odd-mode admittance Y_{odd} at the charge plane $y = y_0$ is given by

$$Y+_{\mathrm{odd},n} = \varepsilon_0 \left(\varepsilon_3 \coth\left(\beta'_n b_3\right)\right) \tag{7}$$

and

$$Y-_{\mathrm{odd},n} = \varepsilon_0 \left(\varepsilon_2 \coth\left(\beta_n b_2\right)\right) \tag{8}$$

where

$$\beta_n = \frac{n\pi}{c}, \qquad \beta'_n = \frac{n\pi}{c'}$$
$$c = 2(d + w) + s$$
$$c' \gg w$$
$$n = 2,\ 4,\ 6, \ldots, \infty.$$

Here, $Y+_{\mathrm{odd}}$ and $Y-_{\mathrm{odd}}$ are the admittances reflected on the charge plane due to the upper layer (ε_3, b_3) and the lower layer (ε_2, b_2), respectively. Using (6)–(8), one can calculate the odd-mode capacitance for the upper and lower layers, respectively. These two capacitances are then summed up. It is important to note that the wall-to-wall spacing for the upper layer is considered to be c', which is much larger than c for the lower layer. Thus, for computation of the upper layer capacitance, one should replace c in (6) by c'.

The odd-mode impedance for the interconnect structure shown in Fig. 5 can now be obtained using the standard formula for characteristic impedance as given in [11]

$$Z_{\mathrm{odd}} = \frac{1}{v^a \sqrt{C_{\mathrm{odd}} C^a_{\mathrm{odd}}}} \tag{9}$$

where superscript "a" denotes free space dielectric.

2) Computation of Even-Mode Impedance: The even-mode admittance Y_{even} at the charge plane $y = y_0$ is given by

$$Y+_{\mathrm{even},n_1} = \varepsilon_0 \left(\varepsilon_3 \coth\left(\beta'_{n_1} b_3\right)\right) \tag{10}$$

and

$$Y-_{\mathrm{even},n} = \varepsilon_0 \left(\varepsilon_2 \coth\left(\gamma_n b_2\right)\right) \tag{11}$$

where

$$\gamma_n = \frac{n\pi}{g}, \qquad \beta'_{n_1} = \frac{n_1\pi}{c'}$$
$$c' \gg w$$
$$n_1 = 1,\ 3,\ 5, \ldots, \infty$$
$$n = 2,\ 4,\ 6, \ldots, \infty.$$

TABLE III
COMPARISONS BETWEEN ANALYTICAL AND SIMULATED RESULTS

Line to line spacing (s) in mm	*Line to center ground spacing (d_1) in mm*	*Simulated (S_{31}) in dB (with center ground track)*	*Analytical (S_{31})in dB (with center ground track)*	*Simulated (S_{31}) in dB (without center ground track)*
0.5	0.1	-18.7	-19.5	-11.1
0.5	0.2	-15.6	-16.7	-11.1
0.75	0.2	-20.4	-19.3	-12.9
0.75	0.3	-17.9	-17.2	-12.9
1.0	0.3	-21.8	-19.2	-14.4
1.0	0.4	-19.9	-18.1	-14.4
1.25	0.4	-23.3	-21.4	-15.9
1.25	0.5	-21.6	-19.6	-15.9

w = 1.5 mm, ε_r = 4.6, b_2 = 1.59 mm, $b_3 \gg b_2$, and d = 50 mm.

TABLE IV
COMPARISONS BETWEEN ANALYTICAL AND SIMULATED RESULTS

Line to line spacing (s) in mm	*Line to center ground spacing (d_1) in mm*	*Simulated (S_{31}) in dB*	*Analytical (S_{31})in dB*
0.5	0.1	-20.3	-21.2
0.5	0.2	-17.1	-17.8
0.75	0.2	-21.8	-20.4
0.75	0.3	-19.5	-18.3
1.0	0.3	-23.6	-21.9
1.0	0.4	-21.6	-20.1
1.25	0.4	-25.3	-23.7
1.25	0.5	-23.4	-20.8

w = 1.5 mm, ε_r = 4.6, b_2 = 1.59 mm, $b_3 \gg b_2$, and d = 0.5 mm.

Again, the even-mode capacitances for the two vertical layers are computed independently. For the lower region (ε_2, b_2), the capacitance is computed using (6) and (11) for even values of "n" since the boundary condition has now changed, whereas for the upper layer, capacitance is computed using (6) and (10). These two capacitances are then summed up.

The even-mode impedance for the interconnect structure shown in Fig. 5 can now be obtained using the standard formula for characteristic impedance as given in [11]

$$Z_{\text{even}} = \frac{1}{v^a \sqrt{C_{\text{even}} C^a_{\text{even}}}}. \tag{12}$$

The voltage coupling coefficient C_v is given by

$$C_v = \frac{Z_{\text{even}} - Z_{\text{odd}}}{Z_{\text{even}} + Z_{\text{odd}}}. \tag{13}$$

The even- and odd-mode propagation parameters for our structure are given by

$$\varepsilon_{f\,\text{odd}}^{\text{even}} = \frac{C_{\text{odd}}^{\text{even}}}{C_{\text{odd}}^{\text{even}\,a}}$$

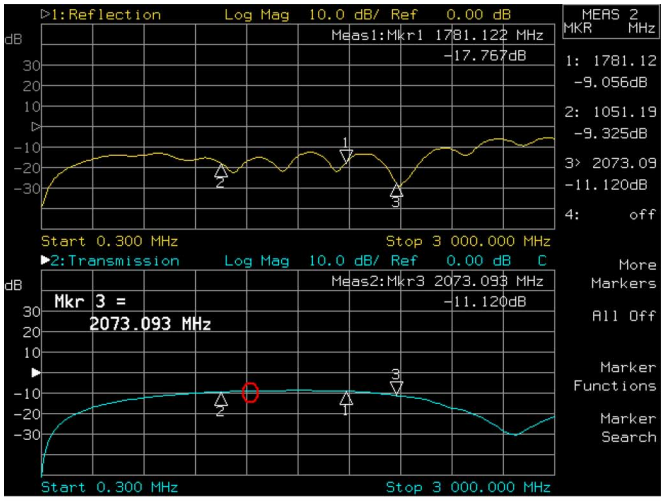
$$\lambda_{\text{odd}}^{\text{even}} = \frac{\lambda^a}{\sqrt{\varepsilon_{f\,\text{odd}}^{\text{even}}}}$$

$$\beta_{\text{odd}}^{\text{even}} = \frac{2\pi}{\lambda_{\text{odd}}^{\text{even}}}. \tag{14}$$

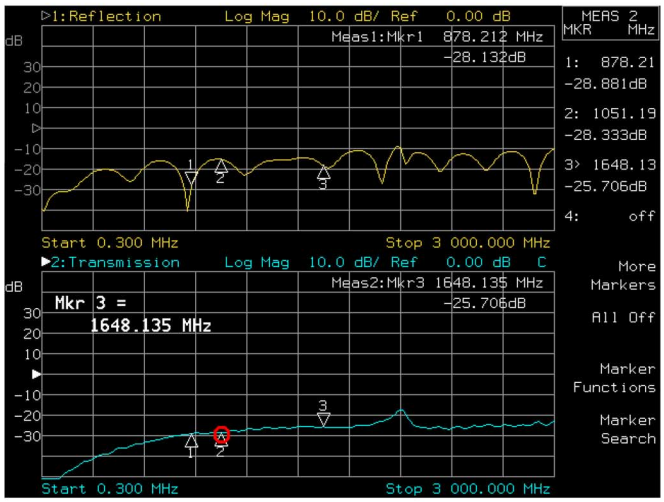
In these formulae, C_{even}, $\varepsilon_{f\,\text{even}}$, λ_{even}, and β_{even} are the capacitance per unit length, effective dielectric constant, guide wavelength, and phase constant, respectively, of the structure in the even-mode excitation, while C_{odd}, $\varepsilon_{f\,\text{odd}}$, λ_{odd}, and β_{odd} are the corresponding parameters in the odd-mode excitation. C^a_{even} and C^a_{odd} are the capacitances per unit length for even- and odd-modes, respectively, when all the dielectrics in the structure are replaced by air. Using the previous formulae, we can compute the capacitive and inductive coupling coefficients as given in [32]

$$k_c = \frac{Z_{\text{even}}\beta_{\text{odd}} - Z_{\text{odd}}\beta_{\text{even}}}{Z_{\text{even}}\beta_{\text{odd}} + Z_{\text{odd}}\beta_{\text{even}}}$$

$$k_l = \frac{Z_{\text{even}}\beta_{\text{even}} - Z_{\text{odd}}\beta_{\text{odd}}}{Z_{\text{even}}\beta_{\text{even}} + Z_{\text{odd}}\beta_{\text{odd}}} \tag{15}$$



(a)



(b)

Fig. 7. (a) Measured and analytical results for coupled lines without ground traces (microstrip coupler) ($w = 1.5$ mm, $b_2 = 1.59$ mm, $s = 0.5$ mm, $\varepsilon_r = 4.6$, length $= 35$ mm). (b) Measured and analytical results for coupled lines with ground traces ($w = 1.5$ mm, $b_2 = 1.59$ mm, $s = 1.5$ mm, $d_1 = 0.25$ mm, $\varepsilon_r = 4.6$, $d = 50$ mm, length $= 35$ mm).

TABLE V
COMPARISONS OF EVEN- AND ODD-MODE IMPEDANCES WITH DESIGN DATA [31]

$w/(b_2 + b_3)$	*Analytical Results*		*Design Data [31]*	
	Z_{even}	Z_{odd}	Z_{even}	Z_{odd}
0.4	107.5 Ω	72.13 Ω	105.15 Ω	69.95 Ω
0.8	68.60 Ω	52.42 Ω	67.20 Ω	50.08 Ω
1.2	50.29 Ω	41.30 Ω	49.34 Ω	39.42 Ω
1.6	39.67 Ω	34.05 Ω	38.98 Ω	32.51 Ω

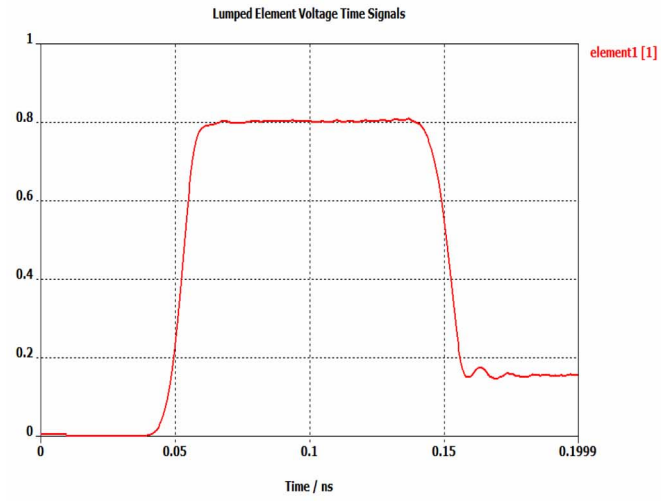
$\varepsilon_r = 2.22$, $b_2 = b_3$, and $s/b_2 = 0.4$.

where k_c and k_l are the capacitive and inductive coupling coefficients, respectively.

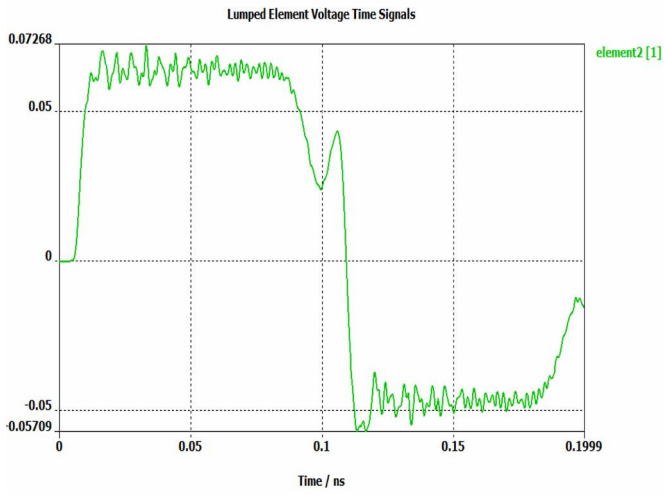
B. Results

While obtaining the simulated results, we have considered 50 Ω terminations at all ends. Table III summarizes the analytical and simulated results for a coupler with centered ground track. From the results presented in Table III, it is seen that the analytical results are within 2 dB accuracy of the results predicted by full-wave simulations. This marginal discrepancy may be attributed to the assumption of converting an inner ground track of finite dimension into an infinitesimally thin vertical ground plane with spacing between the two signal lines altered. The present formulation also leads to interesting insight into the effect of physical placement of ground tracks around the conductors. From Table IV, it is seen that as the lateral walls are placed closer to the conductors, the crosstalk level between the two lines goes down still further. This result provides one more dimension to reduce crosstalk.

The analytical results are also verified by measurements done on a vector network analyzer obtained over a range of frequencies. The measured results are shown in Fig. 7 for two cases: coupled line with and without ground traces between them. The red circles highlight the analytical results. Coupling factors have been measured at a frequency where the length of the



(a)



(b)

Fig. 8. (a) Output voltage response of the driven line (without ground tracks) ($\varepsilon_r = 2.2, b_2 = 0.508$ mm, $w = 0.76$ mm, $s = 0.5$ mm). (b) Voltage coupling at the coupled port of the victim line (without ground tracks) ($\varepsilon_r = 2.2$, $b_2 = 0.508$ mm, $w = 0.76$ mm, $s = 0.5$ mm).

TABLE VI
COMPARISON BETWEEN ANALYTICAL AND SIMULATED RESULTS

ε_2	*Line width (w) in mm*	*Line to line spacing (s) in mm*	*Line to center ground spacing (d_1) in mm*	*Simulate (S_{31}) in dB*	*Analytical (S_{31}) in dB*
2.2	1.2	0.15	0.05	-22.54	-20.96
	1.6	0.25	0.1	-26.7	-24
	1.9	0.35	0.15	-28.93	-27.21
4.6	0.54	0.15	0.05	-17.2	-16.22
	0.62	0.25	0.1	-20.91	-19
	0.86	0.35	0.15	-24.34	-22.47
9.9	0.1	0.15	0.05	-16.11	-13.65
	0.2	0.25	0.1	-18.94	-16.65
	0.28	0.35	0.15	-21.98	-19.17

$b_2 = 0.79$ mm, $f = 7$ GHz, $b_3 \gg b_2$, and $d = 50$ mm.

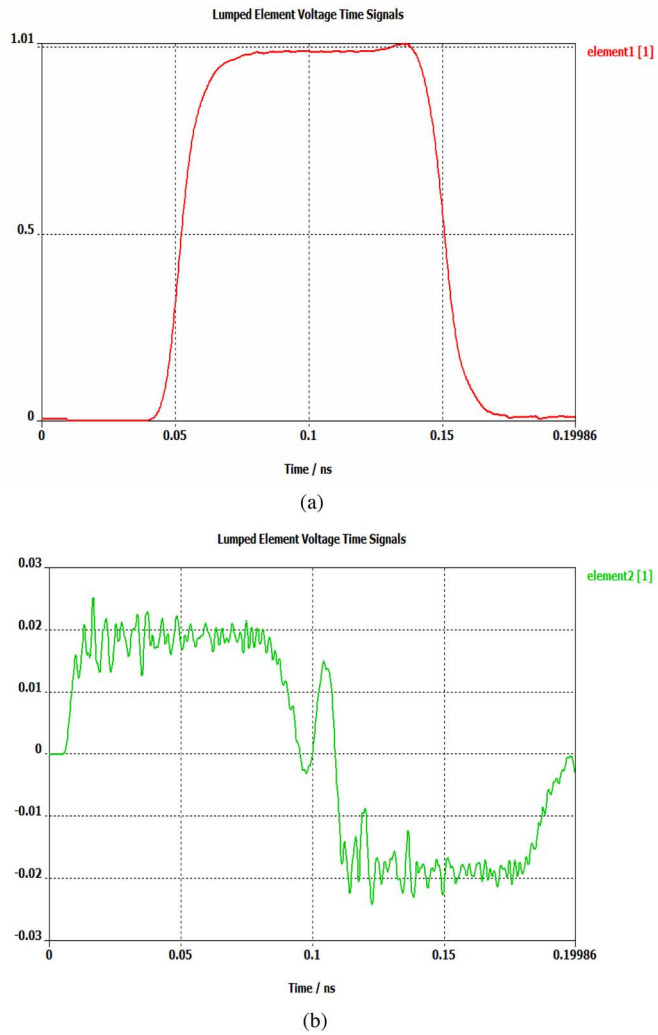


Fig. 9. (a) Output voltage response of the driven line (with ground tracks) ($\varepsilon_r = 2.2$, $b_2 = 0.508$ mm, $w = 0.76$ mm, $s = 0.5$ mm, $d = 0.1$ mm). (b) Voltage coupling at the coupled port of the victim line (with ground tracks) ($\varepsilon_r = 2.2$, $b_2 = 0.508$ mm, $w = 0.76$ mm, $s = 0.5$ mm, $d = 0.1$ mm).

line is equal to $\lambda_g/4$. The computed effective dielectric constant for the coupler with centered ground track is higher than for the conventional microstrip coupler. That is why for the second structure represented by Fig. 7(b), the measurement frequency (denoted by red circle) is lower than that in Fig. 7(a). As a special case, we now compare our results with the design data for a microstrip coupler as given in [31]. The tabulated data in Table V give the results for coupled lines with no ground track between them.

We next perform a time-domain analysis on the structure given in Fig. 5 using FDTD simulations. The input is a unit step pulse (50% duty cycle, 0.2 ns time period, and 0.001 ns rise and fall times), which is fed to the driver line. In the first case, a ground track is not present between the driven and the victim lines, while in the second case, we insert a ground track between the two lines. Figs. 8 and 9 give the output voltage responses of the driven and the victim lines, respectively.

It is clearly seen that the introduction of the ground tracks results in crosstalk minimization. However, the fact that better matching is achieved on the driven line results in almost zero attenuation of the signal at the output end of the driven line. In Section II, we have provided the analysis of line impedance in the presence of grounded tracks. Clearly, the introduction of a ground track between the driven and the victim lines changes the impedance of the driven line. However, care should be taken to properly place this ground track so that perfect matching can be achieved. All this is achieved without any significant penalty on the delay parameters in the driven line. As the ground tracks are placed between the coupled interconnect lines, the placement of ground tracks does not cost much board area. In a way, we can state that it may be possible for a designer to carefully select the distance between the line and the ground tracks so that a 50-Ω line can be fabricated along with superior crosstalk attenuation.

C. Coupling Coefficient Versus Frequency

Table VI gives a comparison between analytical S_{31} and simulated S_{31} for a range of frequencies. The line impedance in all

these cases is 50 Ω and the length of the individual lines is $\lambda_g/4$. The analytical value of coupling coefficient is within tolerable limits when compared to simulated data obtained at 7 GHz. We can therefore infer that the proposed model can be safely used up to 7 GHz.

IV. Conclusion

In this paper, we have proposed closed-form analytical expressions for line impedance and coupling coefficient in the presence of ground tracks. It is shown that the coupling between the driven and victim lines can be reduced along with better matching using the aforementioned analysis. The closed-form expressions will enable designers to strategically place ground tracks on PCBs without any significant penalty in delay or area. The results are valid for a wide range of frequencies that may be of interest for PCB designers, and are verified by simulation and measurements. The proposed model can be modified in future to incorporate the dispersive effects due to open microstrip conditions and the frequency dependence of the loss tangent that is presently beyond the scope of this paper. Formulation is also provided for the calculation of capacitive and inductive coupling coefficients. The novelty of the research lies in the derivation of the admittance parameters for line impedance and coupled lines imposed due to modified boundary conditions, thus retaining the simplicity of the variational analysis for such applications. This study can therefore serve as a good analytical tool for design of high-speed PCB interconnects and dense routing topologies.

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