

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -3 EXAMINATION-October2017

B.Tech/ M.TechI Semester

COURSE CODE: 10M11CH114

MAX. MARKS: 35

COURSE NAME: High Performance Computer Architecture

COURSE CREDITS: 3

MAX. TIME: 2Hr

Note: All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means.

Q1.

[1 x 5 = 5]

- Explain the importance of victim cache?
- What is the advantage of global correlation over predicate bit for dynamic branch prediction?
- Explain the importance of ISA for RISC and CISC architecture?
- What do you mean by graining of a program?
- Explain the importance of benchmark for computer architecture?

Q2.

[Marks 5*2]

- Explain various techniques to reduce the miss penalty and improve the performance of memory architecture?
- You have an L0, L1 data cache, L2 cache, and main memory. The hit rates and hit times for each are: 50% hit rate, 2 cycle hit time to L0. 70% hit rate, 15 cycle hit time to L1. 80% hit rate, 20 cycle hit time to L2. 100% hit rate, 200 cycle hit time to main memory.
 - Find the access time if the data is found in L2 cache.
 - Find the access time if the data is found in L1 cache.
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Q4.

[Marks 5*2]

- Explain the importance of butterfly network over cross bar network and also design butterfly network with 13 nodes and discuss various net performance parameters?
- Explain the importance of scalability in network on chip architecture and discuss 3 type of which are scalable in nature and why? Design omega network for 9 nodes?

Q5.

[Marks 5*2]

- a) Explain what type of programs are best suited for CUDA computing? Explain architectural difference between CPU and GPU with example?
- b) Design a program to convert RGB image to gray scale using CUDA programming? Consider image size 1024×1024 ? Find the speedup over sequential and block size and grid size?

Or

Design a program to for merge using CUDA programming? Consider array size 10^6 ? Find the speedup over sequential, complexity analysis and block size and grid size?