JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -3 EXAMINATIONS-2022

M.Tech-II Semester (ECE)

COURSE CODE (CREDITS): 21M11EC211 (3) MAX. MARKS: 35

COURSE NAME: Digital System Design using Verilog HDL

COURSE INSTRUCTOR: Dr. Pardeep Garg MAX. TIME: 2 Hours

Note: All questions are compulsory. Marks are indicated against each question in square brackets.

Q1 (i). C is a sequential language whereas Verilog HDL is a concurrent language. Justify the concurrent nature of Verilog HDL language with the help of a programming example which uses multiple initial statements and show the output also. **[4 marks]**

Q1 (ii). Clock is a recurring pattern pulse. A clock has to be generated of time period 40 time units which is initialized at time zero and the simulation should finish in 1500 time units. Write a Verilog design code module for the same. **[3 marks]**

Q2 (i). Blocking and Nonblocking assignments can be used in Verilog modules, differentiate between these two by discussing their execution style, operator used etc by taking suitable example. Out of these two, which one is preferred in digital design and why? Which assignment out of these suffers from race condition and which one does not suffer, discuss using a suitable example. **[2+1+2=5 marks]**

Q2 (ii). With few instances, justify under what conditions the usage of for loop is preferred and under what conditions the usage of while loop is preferred. **[2 marks]**

Q3 (i). A J-K flip-flop has to be designed. Write a Verilog design code for J-K flip-flop.

[3 marks]

Q3 (ii). Discuss the usefulness of 'forever' loop in Verilog HDL with the help of a suitable example. **[2 marks]**

Q3 (iii). Describe the significance of sensitivity list/event OR control in Verilog. **[2 marks]**

Q4(i). Write a Verilog design code for 8-bit shift-right-shift-register. **[3.5 marks]**

Q4(ii). A decoder has been designed to decode the input which is 3-bit data. How many unique output lines will be applicable for such decoder? Write a Verilog design code to design this decoder. **[0.5+3=3.5 marks]**

Q5(i). In conditional statements, it is preferred to use if-else loop. The if-else-if loop can be nested also. But, the nested if-else-if loop can become unwieldy if there are too many alternatives. What is the appropriate statement which is preferred in this situation? Discuss that with the help of a suitable example in Verilog HDL. **[3.5 marks]**

Q5(ii). A Verilog design module code is written as follows:

```
reg [15:0] flag;
integer i;
initial
begin
        flag = 16'b 0000_0000_0010_0000;
        i=0;
        begin: block1
        while (i<16)
            begin
                if (flag[i])
                    begin
                        $display("Encountered a True bit at position %d", i);
                        disable block1;
                      end
                    i=i+1;
                end
        end
end
```

What is the special feature which is highlighted in this code, what output will be obtained using this code? Compare the special feature highlighted here with the feature available in C language by discussing its merits. **[3.5 marks]**