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JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -3 EXAMINATION- 2021

B.Tech VII Semester

COURSE CODE: 18B1WEC744 MAX. MARKS: 35

COURSE NAME: FPGA BASED INSTRUMENTATION SYSTEM DESIGN

COURSE CREDITS: 03 MAX. TIME: 2 Hours

Note: *All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means.*

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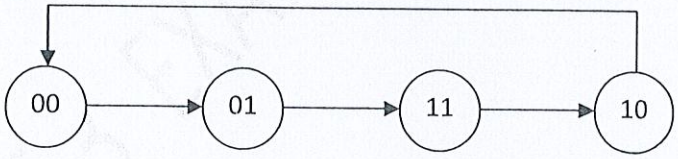
1. Write the behavioural and Gate level Verilog code for 4x1 priority encoder with the given priority $D_3 > D_1 > D_2 > D_0$. [5]
2. Implement $F_1 = AB + A\bar{C}$ and $F_2 = B + \bar{C}$ using PAL, PROM and PLA using minimum possible connections. [5]
3. (a) What do you understand by module instantiation? Explain it with an example. [3]

   (b) Write all the steps for multiplication of $(-4)_{10}$ and $(-5)_{10}$ using Booth's Algorithm. [2]
4. Static Timing Analysis (STA) plays an important role while designing digital circuits. Justify this statement and explain STA in detail. [5]
5. For the following state cycle, design a synchronous circuit using T flip-flop only. [5]



6. Discuss Reconfigurable FPGA-based DSP Systems in detail with its advantages. [5]
7. Find the value of current I flowing through the resistance R_f in the circuit of following DAC. [5]