JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -3 EXAMINATIONS - 2022

B.Tech. VIII Semester (ECE)

COURSE CODE (CREDITS): 19B1WEC831 (03) MAX. MARKS: 35

COURSE NAME: DIGITAL CMOS ICs

COURSE INSTRUCTOR: Dr. SHRUTI JAIN MAX. TIME: 2 Hours

Note: *All questions are compulsory. Marks are indicated against each question in square brackets.*

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1. (*a*) Anu wants to design a 4 × 4 bit NOR-based ROM array. Help her in designing the circuit. Also, make the truth table for the same.

   (*b*) Give overview of semiconductor memory types to Pushp. Also, draw any one equivalent circuit of memory cell. **[2.5 + 2.5 =5]**

2. (*a*) Draw the circuit diagram of the row address decoder for 2 address bits and 4-word lines.

   (*b*) Draw and explain Mahima about one transistor DRAM cell with one bit line and one word line. **[3 + 2 =5]**

3. The average power consumption in conventional CMOS digital circuits can be expressed as the sum of three main components. Elaborate. **[5]**

4. Explain the two circuit design techniques which can be used to overcome the high standby power dissipation? **[5]**

5. (a) Explain the block diagram of an *N* bit number comparator with a gated clock scheme.

   (b) Explain the technique that reduces the energy dissipated during switching events. **[2.5 + 2.5 = 5]**

6. (a) Prove that dissipated energy during charge-up transition is inversely proportional to charging time for Adiabatic Switching.

   (b) What is the role of Hardware Pattern Generator and Output response Compactor in Built-In Self-Test. Explain the architecture of Built-In Self-Test? **[2.5 + 2.5 = 5]**

7. Explain two techniques for each

   (a) On chip clock generation and distribution

   (b) fault types and models controllability and observability **[2.5 + 2.5 = 5]**