JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -3 EXAMINATIONS-2022

B.Tech-VI Semester (ECE)

COURSE CODE (CREDITS): 18B11EC612 (4) MAX. MARKS: 35

COURSE NAME: VLSI TECHNOLOGY

COURSE INSTRUCTORS: ANUJ KUMAR MAURYA MAX. TIME: 2 Hours

Note: *All questions are compulsory. Marks are indicated against each question in square brackets.*

Q1. (a) Draw and explain Y-chart of VLSI design flow introduced by D. Gajski. [02]

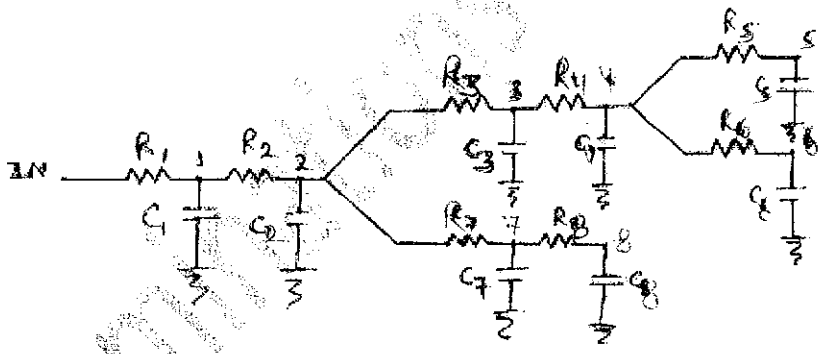
(b) Explain channel length modulation. Also, develop new drain current equation if channel length modulation exists. [03]

Q2. (a) Consider an enhancement type pMOS transistor with following parameters: [03]

$$V_S = 4V, \quad V_G = 2V, \quad V_D = 1V, \quad (W/L)_p = 5,$$
$$V_{SB} = 0V, \quad V_{T0,p} = -0.8V, \quad \mu_p C_{ox} = 100\mu A/V^2.$$

Determine the value of current flowing through this transistor.

(b) Calculate the Elmore delay τ_{D6} at node 6 in the network of Fig. 1. [02]



Q3. Explain the structure and operation of enhancement type nMOS transistor in details. [05]

Q4. Explain CMOS inverter with its circuit diagram, its operation in different operating region and draw its voltage transfer curve (VTC). [05]

Q5. Consider a CMOS inverter with the following parameters: [05]

$V_{T0,n} = 0.6\,V$ $\mu_n C_{ox} = 60\mu A/V^2$ $(W/L)_n = 8$

$V_{T0,p} = -0.8\,V$ $\mu_p C_{ox} = 20\mu A/V^2$ $(W/L)_p = 12$

Find the noise margin NM_H of this circuit. The power supply voltage V_{DD} is 3.3 V.

Q6. Consider a CMOS inverter with the following parameters: [05]

$V_{T0,n} = 1.0\,V$ $\mu_n C_{ox} = 45\mu A/V^2$ $(W/L)_n = 10$

$V_{T0,p} = -1.2\,V$ $\mu_p C_{ox} = 25\mu A/V^2$ $(W/L)_p = 20$

The power supply voltage is 5 V, and the output load capacitance is 1.5 pF. Calculate the fall time (90% level to 10% level) of the output signal.

Q7. Draw the CMOS circuit diagram of two input NAND gate. Explain the working with respect to its truth–table. Also, draw its stick diagram. [05]