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TEST -3 EXAMINATION- December 2021

B.Tech CSE&IT V Semester

COURSE CODE: 18B11CI514 MAX. MARKS: 35

COURSE NAME: COMPUTER ORGANIZATION AND ARCHITECTURE

COURSE CREDITS: 03 MAX. TIME: 2Hr

Note: *All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means.*

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1. Identify the following chips and explain their working:
   (a) 82C59A
   (b) 82C55A
   (c) 8237 **[5Marks]**

2. **(a)** A CPU has a cache of 64 bytes. The main memory has "k" banks, each bank can store "c" bytes of data. The consecutive "c" byte chunks are mapped to consecutive banks with wraparound manner, all k banks can be accessed in parallel. However, the two accesses for the same bank have to be serialized (one after the other). Let "k" equal to 24 and "c" equal to 2. Each iteration requires decoding the bank numbers to be accessed in parallel and this takes about k/2 nanoseconds. Latency of each addressing bank is 80 nanoseconds. How much time is required to transfer the initial block of the cache?

   (b) A CPU has a sixteen-stage pipeline and runs at 2.5 MHz frequency. Instruction fetch happens in the first stage of the pipeline. A conditional branch instruction computes the target address and evaluates the condition in the 15th stage of the pipeline. The processor stops fetching new instructions following a conditional branch until the branch outcome is known. A program executes 1025 instructions out of which 40% are conditional branches. If each instruction takes two cycle to complete on average, then compute the total execution time of the program. **[6 Marks]**

3. **(a)** A computer has a 256 KByte, 4-way set associative, write back data cache with block size of 32 Bytes. The processor sends 32 bit addresses to the cache controller. Each cache tag directory entry contains, in addition to address tag, 2 valid bits, 1 modified bit and 1 replacement bit. Compute the number of bits in the tag-field of the address as well as the size of tag-directory.

   (b) Multiply (-10) and (-4) using Booth's algorithm. Assume the size of the register to be 4. **[6 Marks]**

4. **(a)** Suppose that a system is being designed with the perception of direct communication between I/O and main memory without involving the CPU, what could be the possible solution to achieve this?

   (b) If we use 3-bits in the instruction word to indicate if an index register is to be used and if necessary, then which one is to be used, then find the maximum number of index registers to be used in the machine? **[6 Marks]**

5. **(a)** An instruction is stored at location X with its address field at location X+1. The address field has the value Y. A processor register contains the number Z. Evaluate the effective address is the following instruction modes are used:
   1) Direct.
   2) Immediate.
   3) Relative.
   4) Register Indirect.

   (b) Pick up the correct RAID level with the following requirements.
   1) Which supports two disk failures simultaneously?
   2) Number of disks required in "Redundant data with hamming code".
   3) Most expensive level. **[6 Marks]**

6. **(a)** Represent 1.1010001 in floating point representation with 8 exponent bits and 23 mantissa bits?

   (b) Specify the lower and higher range for the same format.

   (c) Specify the reason, why exponent is present before mantissa (significant) in the format.

   (d) In exponent the biased representation is used, specify the reason? **[6 Marks]**