Mr- Akhil Ranjan.

JAYPEE UNIVERSITY OF INFORMATRION TECHNOLOGY, WAKNAGHAT

MID SEMESTER EXAMINATION-2015

B.Tech VIIIth Sem And M.Tech 2nd Sem, ECE

COURSE CODE: 10M21EC211 MAX. MARKS: 30

COURSE NAME: Advanced CMOS Digital Design Techniques

COURSE CREDITS: 03 MAX. TIME: 2 HRS

Note:- All Questions are compulsory.

Section A (1*6 = 6 Marks)

1> i> Resistance per unit length for a 3 cm long and 8 cm wide wire is 0.06 ohm/μm. Find sheet resistance of the wire.

ii> Explain the consequences of inductive effects of wire.

iii> How the Manhattan style of routing leads to the improvement of performance of any circuit.

iv> Nowadays, which material is replacing Aluminium as the interconnect material. Mention its advantages.

v> Two systems are accessing a single resource. Both have sent active high signal at the same time. Which circuit is used to solve this deadlock? Explain the working of the circuit.

vi> Draw Truth Table of Muller-C-Element. Implement this logic using CMOS.

Section B (3*3 = 9 Marks)

2> There is a circuit which generates a single pulse of pulse width 4 ns. Implement this circuit using TSPC Logic.

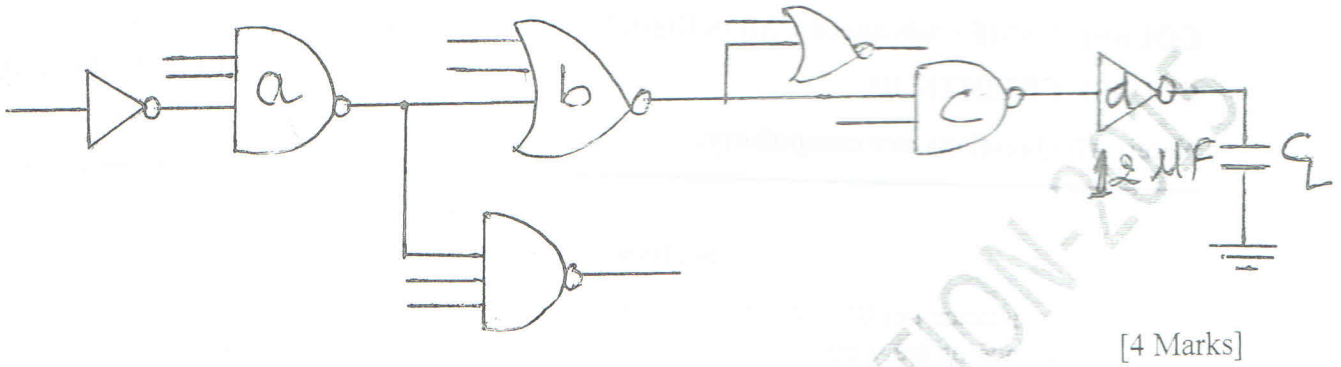
3> What is the impact of overlapping clock? With suitable diagrams, explain the working of any circuit which is insensitive to clock overlaps.

4> Explain the working of a circuit which generates a glitch signal around negative edge of the clock. Assume propagation delay of a gate= 1ns * no. of inputs. Use a maximum of 4 logic gates in the circuit.

P.T.O

Section C (15 Marks)

5> Find the size of a, b, c, d with respect to the size of 1st gate in order to minimize the propagation delay for this complete logic chain. Input capacitance of 1st gate is 2 μF.



[4 Marks]

6> Explain the working of a specialized negative edge triggered D Flip-Flop using TSPC logic. (Circuit should not have the combination of positive latch and negative latch.)

[4 Marks]

7> Design a circuit which will give the same output as Negative edge triggered JK Flip-Flop when both inputs of Flip-Flop are 1. Clock waveform toggles after every 5 ns. Any combinational logic used in the circuit is having a propagation delay equal to the half Time Period of the clock.

[3 Marks]

8> a> Explain the term progressive transistor sizing and input re-ordering. Explain how it minimizes the propagation delay of any circuit.

b> Resistive parasitic effect degrades the signal level. Explain its impact on the working of a CMOS inverter. Suggest a possible solution to this problem.

[2+2= 4 Marks]

**********The End**********