Prof. Meenakshi Sood.

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT
END SEMESTER (MAY 2015)
B. Tech. 4th Semester (ECE)

COURSE CODE: 10B11EC401 **MAX. MARKS: 45**
COURSE NAME: DIGITAL ELECTRONICS **MAX.TIME:3 HRS**
COURSE CREDITS: 4

Note: *All questions are compulsory.*

Section A

(Marks: 10)

1. How many bits are required for designing a converter, which has resolution of 5mV and the ladder has full scale +8V.
2. Explain the terms: Fan-out Tri-state gates for logic families.
3. Draw the circuit of CMOS inverter.
4. Convert $(678)_9$ into Gray code.
5. Draw the circuit diagram of Bi-stable multivibrator.
6. Define the Reflected code with example.
7. In the following series, the same integer is expressed in different number systems. Determine the missing member of the series.10 000, 121, 100, ? , 24, 22, 20, . . .
8. Determine the possible base values $(123)_x + (543)_x = (666)_x$
9. Draw the Full Adder circuit using AOI logic.
10. Simplify the Boolean expression: $w'x' + x'y' + w'z' + yz$

Section B

(3*5 = 15Marks)

B.1 *(a)* Draw the logic diagram of a four bit bidirectional shift register with four D flip flops and four 2:1 multiplexers.

(b) What is Race around condition in flip flops? Explain the logic behind Master- Slave FF.

B.2 *(a)* A sequential circuit uses two JK flip-flops as memory elements. The behavior of the circuit is described by the following equations: Derive the state table and draw the state diagram of the circuit.

$J_0 = X'$ $K_0 = X$

$J_1 = Q_1 X$ $K_1 = Q_0x' + Q_0x$

$Y = Q1\ Q_2$

(*b*) Design a full subtractor using 4:1 MUX.

B.3 (*a*) Draw the logic diagram of a 3-input TTL NAND gate and explain its working .

(*b*) Design a combinational circuit with three inputs and three outputs. When the binary input is 0,1,2,3, the binary output is one greater than the input. For rest of the inputs the value is one less than the input.

Section C

(4*5 = 20 Marks)

C.1 Generate the saw-tooth waveform having duty cycle at least 60% using IC 555.

C.2 Design a four bit, J-K counter having the output sequence is {0, 2, 4, 6, 8, 10, 0, 2, 4…….} with a synchronous clear.

C.3 Design an 5-4-2-1 to 8-4-2-1 code converter using

a. ROM

b. PLA

C.4 Implement the following multiple output using a 4-line to 16-line decoder:

$$F_1 = \sum m(0,1,4,7,12,14,15)$$

$$F_2 = \sum m(1,3,6,9,12)$$

$$F_3 = \sum m(2,3,7,8,10)$$

$$F_4 = \sum m(1,3,5)$$

C.5 Explain the Flash and Successive- Approximation A/D converter and compare its specifications?

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