Dr. Shruti Jain (ECE)

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

SUMMER SEMESTER (JULY 2016)- B-Tech
END TERM EXAM

COURSE CODE: 10B11EC612 MAX. MARKS: 50
COURSE NAME: VLSI Technology and Applications MAX.TIME: 2 HRS
COURSE CREDITS: 4

1. Derive the pull up and pull down ratio for an *n*MOS inverter driven by another *n*MOS inverter.

2. Consider the following parameters for *n*- channel enhancement type MOSFET having grading coefficient for junction as 0.4, Substrate doping = 3×10^{12} cm^{-3}, Source/Drain doping = 10^{19} cm^{-3}, gate oxide thickness = 40 nm, junction depth= 1.2 μm, length of drain = 9μm, width = 4μm. If drain voltage is 4V, find drain-substrate diffusion capacitance.

3. Consider a resistive load inverter circuit with V_{DD} = 5V, $k`_n$ = 20μA/V^2, V_{T0} = 0.8V, R_L= 200KΩ, W/L = 2. Find the high state and low state noise margin of the circuit.

4. Explain the different steps of fabrication of *n* type Enhancement MOSFET.

5. Sketch the CMOS logic circuit and stick diagram that realizes the two input NAND gate.