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## JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

## TEST -1 EXAMINATION- September 2016

M.Tech I Semester (ECE)

COURSE CODE: 10M11EC114

MAX. MARKS: 15

COURSE NAME: VLSI CIRCUIT AND SYSTEM DESIGN

COURSE CREDITS: 04

MAX. TIME: 1Hr

Note: All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means.

- 1. Consider an enhancement MOS system with the following parameters:  $t_{ox} = 200$ Å,  $\phi_{GC} = -0.85$ V,  $N_A = 2.10^{15}$ /cm<sup>3</sup>,  $Q_{ox} = 2q.10^{11}$  C/cm<sup>2</sup>. [3 + 2 = 5]
  - a) Determine the threshold voltage  $V_{T0}$  under zero bias at room temperature.
  - b) Determine the type (p type or n type) and amount of channel implant (/cm²) required to change the threshold voltage to 0.8V
- 2. a) A n MOS transistor with  $V_A = 100 \text{ V/} \mu\text{m}$  is operated at a dc current  $I_D = 1 \text{ mA}$ . If the channel length is doubled and  $V_{GS}$  is fixed, find the new values of  $\lambda$ ,  $V_A$ ,  $I_D$ , and  $r_o$ .

 $[0.5 \times 4 = 2]$ 

- b) A p MOS transistor has  $k_p$  (W/L) =  $80\mu$ A/V<sup>2</sup>,  $V_{th}$  = -1.5V, and  $\lambda$  = -0.02V<sup>-1</sup>. The gate is connected to ground and the source to + 5V. Find the drain current for  $V_D$  = +1.5V. Also find the effect of both scalings on the drain current if scaling factor is 2. [1 + 1 + 1 = 3]
- 3. The process parameters are:  $N_{\rm D} = 2 \times 10^{30}$  cm<sup>-3</sup>,  $N_{\rm A} = 1 \times 10^{15}$  cm<sup>-3</sup>,  $x_{\rm j} = 0.5$  µm, W = 10 µm, Y = 6 µm,  $t_{\rm ox} = 0.05$  µm,  $V_{\rm TO} = 0.8$ V, channel stop doping = 16 × (p- type substrate doping). Find the effective drain parasitic capacitance when the drain node voltage changes from 5V to 2.5V.