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JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST-3 EXAMINATION- JUNE -2016

B. Tech 8th Semester

(Electronics and Communication Engineering)

COURSE CODE: 11B1WEC232 MAX. MARKS: 35

COURSE NAME: SOFTWARE DEFINED RADIO

COURSE CREDITS: 03 MAX. TIME: 2 HRS

Note: *All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means.*

Q. 1(a) What are the digital signal processing hardware issues? Discuss any one potential issue in details. **[4]**

(b) Why is it desirable to use direct conversion receiver to implement an array? **[3]**

Q. 2(a) What features do FPGA have that are beneficial for the software defined radio implementation? **[4]**

(b) What are the advantages of FPGA as compared to DSP and ASIC? **[3]**

Q. 3(a) What is the dynamic range? Discuss its principal challenges of dynamic range of a software defined radio receiver design. **[4]**

(b) What is the CORBA? What is its role in software defined radio? **[3]**

Q. 4(a) What is the drawback of Direct Digital Synthesizer systems and how can hybrid systems help to combat this drawback? **[4]**

(b) What is the CORDIC algorithm and how is it used to perform Direct Digital Synthesis in software defined radio? Explain with suitable diagram. **[3]**

Q. 5(a) What is the benefit of using the multi-stage (rather than single stage) structures of a decimator or interpolator when large changes of sampling rate are required? **[4]**

(b) Why is it important for the RF components in an antenna array to have uniform characteristics across the channel? **[3]**