

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

T -3 EXAMINATION (JUNE 2016)

B.Tech 4th Sem. (ECE)

COURSE CODE: 10B11EC411

Max Marks: 35

COURSE NAME: Semiconductor Devices

Max Time: 2hrs.

COURSE CREDITS: 4

Note: All questions are compulsory. Carrying mobile phone during examination will be treated as case of unfair means. Attempt all parts of question at one place.

Q1. All questions carry one mark

[1x10]

- i. Why a pure semiconductor does behave like an insulator at absolute zero temperature?
 - ii. Define electron affinity.
 - iii. Why the energy gap between the valance band and the conduction band is known as forbidden energy gap?
 - iv. Which of the two semiconductor materials, Si or Ge has larger conductivity at room temperature and why?
 - v. Write down the condition to make an ohmic contact between metal and semiconductor.
 - vi. What is step junction?
 - vii. Name the factors which make the JFET superior to BJT.
 - viii. Define average life time of a carrier.
 - ix. Define threshold voltage for MOSFET.
 - x. What is the difference between elemental and compound semiconductors?
- Q2.** Derive diode equation $I = I_0 \left(e^{\left(\frac{qV_{EB}}{KT} \right)} - 1 \right)$, where I_0 is the reverse saturation current. **[5]**
- Q3.** With reference to the working of MOS capacitor explain in detail the meaning of **[5]**
 (a). Accumulation
 (b). Depletion
 (c). Inversion
- Q4.** What do you understand by a rectifying contact and how do you proceed to make a rectifying contact between metal and N- type semiconductor? **[5]**
- Q5.** A Si PNP transistor at 300k has $N_{oe} = 2 \times 10^{18}/\text{cm}^3$, $N_{db} = 10^{17}/\text{cm}^3$ and $N_{oc} = 10^{16}/\text{cm}^3$. assume an effective cross section area A is 10^{-4}cm^2 , base width is $1\mu\text{m}$ and minority carrier diffusion length for electrons and holes is $10\mu\text{m}$. $D_b = 5\text{cm}^2/\text{sec}$, $D_e = 20\text{cm}^2/\text{sec}$. Calculate I_e , I_c and α for forward active mode and $I_b = 2\mu\text{A}$. **[5]**
- Q6.** Calculate and plot the excess hole distribution $\delta(p_n)$ in the base of PNP transistor assuming $w_b/L_p = 1$ and $w_b/L_p = 0.2$. Also assume that the collector base junction is strongly reversed biased. **[5]**