Dr. Pardeep Kumar

JAYPEE UNIVERSITY OF INFORMATION TECNOLOGY

T1 EXAMINATION 2016

M.Tech 1st Sem / B.Tech 7thSem

COURSE CODE: 10M11CI114 **MAX. MARKS: 15**

COURSE NAME: High Performance Computer Architecture **MAX. TIME: 1 HRS**

Note: All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means.

Q1. **[1 x 5]**

a. What is the importance of interconnected network over simple network?
b. How does data dependency affect the performance?
c. If a processor P1 has 2 GHz and P2 has 1.5 GHz and CPI of program1 on P1 and P2 are given as 5 and 4 instruction, which processor has higher speed up?
d. What do you mean by graining of a program?
e. Explain the importance of ISA for RISC and CISC architecture?

Q2. Design a pipeline for given set of instructions with and without forwarding? Find CPI and average CPI for set of instruction given below? **[4 Marks]**

-Where
SUB takes 3 clock cycles
ADD takes 2 clock cycles
MUL takes 2 clock cycles

LW R1, 4
SUB R4, R1, R9
ADD R2, R4, R9
ADD R1, R2
MUL R4, R1

Q3. Explain flying classification for computer architecture? Discus disadvantages of flying taxonomy over shared memory architecture? **[2 Marks]**

Q4. Explain different parameters to study the performance of computer architecture? **[2 Marks]**

Q5. Assume that a divide instruction take 10 cycles and contributes to 20% of the instructions in a program, 25 % of instructions are ADD/SUB type which takes 2 cycles and remaining 55% of the instruction requires an average of 3 cycles. **[2 Marks]**

a) What percentage of CPU spends on division?
b) If divide instruction cycles would be reduced to 8 cycle with 15% increase in the cycle time. Find the speedup and should we proceed with the modification?