ANALYTICAL STUDY OF THE PULSE-SHAPING AND FREQUENCY ALLOCATION FOR SOFTWARE DEFINED RADIO

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ANALYTICAL STUDY OF PULSE-SHAPING AND FREQUENCY ALLOCATION FOR SOFTWARE DEFINED RADIO

by

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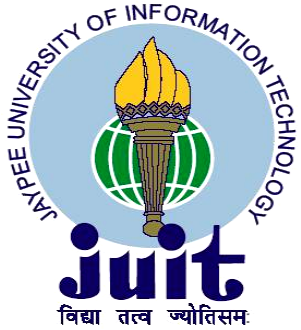

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CERTIFICATE

This is to certify that the thesis entitled, "**ANALYTICAL STUDY OF PULSE-SHAPING AND FREQUENCY ALLOCATION FOR SOFTWARE DEFINED RADIO**" which is being submitted by **Mr. AJAY KUMAR SINGH** in fulfillment for the award of degree of Doctor of Philosophy in **COMPUTER SCIENCE AND ENGINEERING** by the Jaypee University of Information Technology, is the record of candidate's own work carried out by him under my supervision. This work has not been submitted partially or wholly to any other University or Institute for the award of this or any other degree or diploma.

Dr. G. Singh
(Associate Professor)

(Supervisor)

Dedicated to

My family. . . .

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LIST OF PUBLICATIONS

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2. **Ajay K. Singh,** P. Kumar, G. Singh and T. Chakravarty, "Linearizer for pulse-shaping of received pulse in ultra-wideband radio systems," Digital Signal Processing, vol. 20, no. 2, pp. 496-501, March 2010.
3. **Ajay Kr. Singh**, G. Singh, Ved. P. Mishra and Ankita Taneja, "Frequency allocation in software defined radio using smart cards," Electronics For You, vol. 40, no. 10, pp. 108-114, Oct. 2008.
4. **A. K. Singh,** G. Singh and D. S. Chauhan, "Implementation of Real Time Programs on the TMSC6713DSK Processor," Int. Journal of Signal and Image Processing, vol. 1, no. 3, pp. 160-168, May 2010.

Conference

1. Ankita Taneja, Ved. P. Mishra, **Ajay Kr. Singh,** G. Singh and S. P. Ghrera, "Security architecture for SDR system using OTA download sequence," Proc. Technical Conf. and Product Exposition, SDR 08, Washington DC, USA., Oct. 26-30 2008.
2. **Ajay Kr. Singh,** G. Singh and D. S. Chauhan, "Software defined radio in wireless ad-hoc network," Proc. Technical Conf. and Product Exposition, SDR 08, Washington DC, USA., Oct. 26-30, 2008.
3. **Ajay Kr. Singh**, Ankita Taneja, Hemant Tandon, Ankur Aggarwal and G. Singh, "Software Defined Radio ─ Talk Through Application," Proc. IEEE Int. Conf. Recent Advances in Microwave Theory and Applications, pp. 821-824, 21-24 Nov. 2008.
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LIST OF ABBREVIATIONS

ADC - Analog-to-Digital Converter

AGC - Automatic Gain Control

AI - Artificial Intelligence

ASIC - Application Specific Integrated Chip

BER - Bit Error Rate

CCI- Co-Channel Interference

CDMA - Code Division Multiple Access

CIR- Carrier-to-Interference Ratio

CORBA - Common Object Request Broker Architecture

CPU - Central Processing Unit

DAC - Digital-to-Analog Converter

DBMS - Database Management System

DC - Direct Current

DDS - Direct Digital Synthesizer

DSK - Digital Signal Processing Starter Kit

DSP - Digital Signal Processing

DTR - Data Terminal Ready

DXR - Data Transmit Register

EDMA - Enhanced Direct Memory Access

EEPROM - Electrical Erasable Programmable Read Only Memory

FCC - Federal Communications Commission

FFT - Fast Fourier Transform

FIR - Finite Impulse Response

FPGA - Field-Programmable Gate Array

GSPS - Giga Sample Per Second

giga-FLOPS - giga Floating Point Per Second

I/Q - In-phase/Quadrature

IF - Intermediate Frequency

ISI - Inter-Symbol Interference

LNA - Low Noise Amplifier

LO - Local Oscillator

LPF - Low Pass Filter

McBSP - Multichannel Buffered Serial Port

MPSK - M-ary phase shift keying

MSE - Mean-Square-Error

NCO- Numerically Controlled Oscillator

NVM - Non-Volatile Memory

OTA - Over-the- Air

PCI - Peripheral Computer Interconnect

PCM - Pulse Coded Modulation

PDC - Programmable Down Conversion

PIN - Personal Identification Number

PRF - Pulse Repetition Frequency

RF - Radio Frequency

SCA - Software Communications Architecture

SDR - Software Defined Radio

SNR - Signal-to-Noise Ratio

SPI - Serial Peripheral Interface

TDMA - Time Division Multiple Access

TGC - Transmit Gain Control

UWB - Ultra Wide Band

VGA - Video Graphics Array

VLIW - Very Long Instruction Word

YIG - Yttrium Iron Garnet

ABSTRACT

The exponential growth in the ways and means by which people need to communicate, modifying radio devices easily and cost effectively has become a potential issue. The hardware based radio device limits cross-functionality and can be modified through physical intervention. This results higher production cost and minimal flexibility in supporting multiple wave standards.

In contrast, software defined radio (SDR) technology provides an efficient and comparatively inexpensive solution to these problems and allowing multimode, multi-band and multi-functional wireless device that can be enhanced by using software updates. These devices include field-programmable gate array (FPGA), digital signal processing (DSP), general-purpose preprocessor (GPP), system-on-a-chip (SoC), or other application specific programmable processors with the use of these technologies, which allows new wireless features and capabilities are to be added to the existing radio system without requiring new hardware. By simply downloading a new program, the software radio is able to interoperate with different wireless protocols, incorporate new services and upgrade to new standards. Thus, the SDR is a radio communication system which can tune to any frequency band and receive any modulation across a large frequency spectrum by means of programmable hardware which is controlled by software. This means that the frequency band, performance and functionality can be upgraded with a simple software download and update. It is important to note that SDR is not confused with application software and other software not associated with radio. It provides an efficient and comparatively inexpensive solution to the problem of building multimode, multiband, multifunctional wireless devices.

SDR architectures include transceivers that perform up-conversion and down-conversion between baseband and radio frequency (RF), exclusively in the digital domain, reducing the RF interface to a transmit-channel power amplifier, low-noise amplifier for the receive path, and minimal analog filtering. The major challenges in the SDR are pulse shaping, digital beamforming, frequency allocation,

reconfigurability with channelization and communication security. In this thesis, we have tried to overcome the aforementioned mentioned potential challenges.

The organization of thesis is as follows: Chapter 2 emphasizes on the pulse shaping by linearization technique. As we know, the power amplifier is a key element in every radio communication system, and is required to serve the function of amplifying the information-bearing signal, without distortion, with an efficient manner. However, the distortion in power amplifiers occurs in different ways, such as nonlinear distortion and temporal linear dispersive frequency. Hence, we have discussed a linearization technique for pulse shaping of the received pulse. RF linearization techniques, which enable a balance to be made between the efficient power amplifiers and modulation methods. Here we present a novel concept of pulse-shaping in an ultra-wideband (UWB) radio system. Instead of attempting to design an antenna with flat group delay, the emphasis has been shifted to the signal processing aspect of pulse-shaping. The received pulse, which has broadened due to dispersive phase response of the propagating channel, is shaped back closer to the ideal pulse using a linearizer.

Chapter 3 concerns with the digital beamformer with low angle resolution. The digital beamforming is becoming an important tool in the communications for the system improvement of the quality of service and network capacity. In the receive mode, the digitized radio returns weight and is allocated in such a way that the first pulse reflect a SUM pattern and the subsequent three pulses reflect DIFFERENCE pattern. The pulses on DIFFERENCE pattern are added to each other and the net signal is subtracted from the signal received in SUM pattern. This results in a very narrow beam which shows narrow spatial resolution.

Chapter 4 investigates the frequency allocation in the SDR using smart cards. The portability of software for every frequency that has to be received using an SDR, keeping in mind the security-concerns is a major issue for discussion these days. We must also notice that the particular features of flash memories make smart card databases differ from main memory databases, where flash memory acts as a true secondary storage with very different read/write proprieties with respect to RAM the main memory, making it look more like a traditional data base management system (DBMS).

Chapter 5, concerns with the real-time implementation of program using TMS320C6713DSK Processor. Here, first we have configured multichannel buffered serial port (McBSP) by using code composer written in C language. We made our own hardware and interfaced it with DSP Kit and CRO to see the output. We got the output even by four times overlapping, obviously by maintaining Nyquist criterion.

In Chapter 6, we aimed at validating the functioning of Wireless Ad-Hoc Network with SDR. The parameters of communication in an ad-hoc networks changes frequently such as the distance between nodes, channel characteristics and person who is using it. We can change software specification rather than changing any hardware such as chip every time. Change of hardware leads to the wastage of money. In this way the SDR is economically beneficial to us. Finally,

Chapter 7 concludes the thesis and proposes possible future direction of the research.

CHAPTER-1

INTRODUCTION

1.1 Basic Concept of the Software Defined Radio

One of the recent and interesting evolutions in the wireless communications area is the trend toward the integration of multiple functions. The communications (Lang et al, 2004) industry is seeking to create radios that can handle multiple frequency bands, use multiple transmission protocols and are reconfigurable, preferably on-the-fly. Software Defined Radio (SDR) (Walter Tuttlebee and Walter H. W. Tuttlebee, 2002) is a concept that has been giving momentum in realizing a wireless multi-mode, multi-band, multi-standard radio terminal capable of operating according to variety of different mobile communication standards (Mitola, April 1999). It is an emerging technology that is profoundly changing the radio system engineering. Just as its name implies, SDR system is a radio communication system which can tune to any frequency band and receive any modulation across a large frequency spectrum by means of a programmable hardware which is controlled by software. By simply downloading a new program, a software radio is able to interoperate with different wireless protocols, incorporate new services, and upgrade to new standards. The need to communicate with people using different types of equipment can only be solved using software programmable radios because of its flexible architecture. Thus, the SDR is also called software radio, refers to wireless communication in which the transmitter modulation is generated or defined by computer. Software defined radio (Reed, 2002) is a promising technology, which facilitates wireless system configuration and development. These systems provide three key advantages over traditional 'hard-wired' radios:

- Provide low-cost solutions, since functionality that used to be hard-wired into the radio can now be provided via software
- Are easy to upgrade either by a physical connection or even remotely, that is, over-the-air, by radio transmission

• Potentially allow a faster evolution of industry standards, end-user equipment and communication and network infrastructures.

In addition, there are issues arising from the considerable strain on existing bandwidth and infrastructures from the growing number of mobile and wireless devices (Stenumgaard, 2006). With ever increasing numbers of users requiring access to different parts of the spectrum, it is hard to envisage that any of these issues can be solved with conventional, inflexible hard-wired radio systems.

Problems resulting from having multiple frequency bands as well as different communication standards make it impossible for the current generation of analog systems to interoperate. Providing all signals processing in software by converting received signals into digital form immediately after an antenna which produces a new qualitative leap in frequency agility as well as protocol standard independence. It solves the problem of system interoperability in a highly fragmented communication environment (Harada and Prasad, 2002). However, to realize all the potential benefits of direct conversion radio a few vital signal processing problems originating from the specifics of software radio have to be addressed. The software radio has emerged from theoretical research as a commercially viable and flexible digital communication system. Advances in digital technology are quickly making the software radio an attractive strategy for low-cost multi-dimensional transceivers (Rykaczewski et al, 2008). In the software radios a relevant problem is the down-conversion with high image frequency suppression. For this purpose, a down-converter has been developed utilizing a signal processing method along with the homodyne reception principle. A simplified system has been built to test this new method. For comparison the development of intermediate frequency digital sampling approach is in progress.

The software radio tends to use simpler radio frequency hardware with more complex controlling software that is achieved by a highly sophisticated digital signal processing technique. The optimal border-line for the interface between the hardware and software is to be investigated. Several functions can be realized by combining analog and digital circuitry with controlling software. The analog circuitry of a software radio has to reflect the demands for an easily reconfigurable transmission system (Baines and Pulley, 2003). This flexibility is a very relevant property of the software radio, because with this the compact implementation of a multi-standard

system is realized. It means the frequency allocation of the transmitted channels, the modulation format and the modulation bandwidth (Peek, 2005) should be changeable according to the information content. The other important quality is the reprogrammability (Saha and Sinha, 2008). Finally, the highly competitive marketplace needs low cost, high efficiency multi-channel and multi-standard systems.

A convergence is occurring in radio communications through DSP (Sala et al, 2004) software to perform most radio functions at performance levels previously considered unattainable. DSP has now been incorporated into much of the amateur radio gear on the market to deliver improved noise-reduction and digital-filtering performance. SDR and especially it's most advanced implementation based on the direct RF conversion to baseband has brought us to the verge of revolution in communication. These systems are potentially capable to solve system interoperability problem by providing seamless system operation in highly fragmented, multi-terminal/multi-frequency communication environments typical for today communication (Irmer, 1986). All essential signal and data processing functions in such systems are performed in software providing reconfigurability essential for multimode/multi-terminal operation. Achieved system flexibility includes provision for interoperability and "on the fly" reconfiguration from individual radios to the entire radio system. Interoperability by itself is defined as the ability to share information between different users or systems via voice or data signals in real time, when needed, and as authorized. Potentially, another important feature of software radios is its ability to respond to changes in operating conditions by, for example, changing their modulation schemes, rather than having a circuit that generates a particular fixed waveform, a more flexible radio could synthesize the waveform required for a particular set of conditions. A radio that generates and detects many types of waveforms could operate in a much broader range and environmental conditions.

With the emerging concept of SDR, new flexible platforms seem to be at hand, capable not only of providing a reprogrammable hardware platform but also of supporting the various needs of an optimal adaptive algorithm for pre-distortion. In particular, those hardware architectures that are flexible during run-time are of

particular interest for SDR as well as for adaptive pre-distortion techniques. Since such techniques require sophisticated algorithms running permanently to adapt to continuously changing behaviors, it is of the utmost importance to have hardware architectures available that are as optimal as possible in order to achieve the best results with the lowest complexity. The emerging concept of SDR enables new flexible platforms, capable of providing reprogrammable hardware and supporting optimal adaptive algorithm for pre-distortion. The optimal algorithm for adaptive RF linearization is not known. This field is relatively new and much is in progress and in movement. It is very likely that there will be different algorithmic techniques depending on the mode of operation rather than a single one. It is the staggering rate at which the speed of processors and DSP (Jeckeln et al, 2004) components has increased that has led to the realization of SDR concepts. The reconfigurable DSP core allows the processing functions to be easily changed on-the-fly to incorporate different functionality as required. Conversely, it is not so straightforward to integrate the same level of reconfigurability into the RF amplification and the up and down conversion stages. However, recent advances in analogue-to-digital and digital-to-analogue converters (ADCs and DACs, respectively) have made it possible to directly convert signals closer to the antenna, at high speed and with increasing dynamic range. This is a huge step towards a completely digital solution and consequently optimal flexibility. A number of issues associated with the main components of SDRs are discussed briefly below.

Software radio (Yang et al, 2001) offers the advantages of putting many traditionally hard functions in modules whose characteristics can be changed while the radio is running. For example, rather than tuning a circuit to filter (Hontsu et al, 2005) a certain frequency band, developers can use software to provide more flexible filtering that could change as the radio operates (Shah, 2002). The software radio architecture centers on the use of wide ADC and DAC converters as close to the antenna (Mattioniv and Marrocco, 2007) as possible, with as much radio functionality as possibly defined in software. Although, the software radio use digital techniques, software controlled digital radios are generally not software radios. The key difference is the total programmability of software radios (Shono et al, 2005), including programmable RF bands, channel access modes, and channel modulation.

The software radio architecture (Eyermann and Powell, 2001) is widely applicable to radios, peer networks, air and sea traffic management, mobile military communications (Krawczyck, 2001), and satellite mobile systems. The software radio has the potential to reduce the size, complexity and power of consumption of a radio system (Mitola Joseph III). More importantly, because processing is done in software, it has the potential to be amazingly versatile, allowing a single system to have a range of applications. The key techniques related with software radio include bus standard (Hamabe et al, 1988), wide band antenna, (Mattioni et al, 2008) high speed and parallel processing of (Singh et al, Nov. 2008) DSP, and so on.

In essence, an SDR is a radio that is substantially defined in software, with a physical layer (McClelland, 1983, Knight and Lewis, 2004, Huang and Kung, 1997) behavior that can be significantly altered through changes to its software.

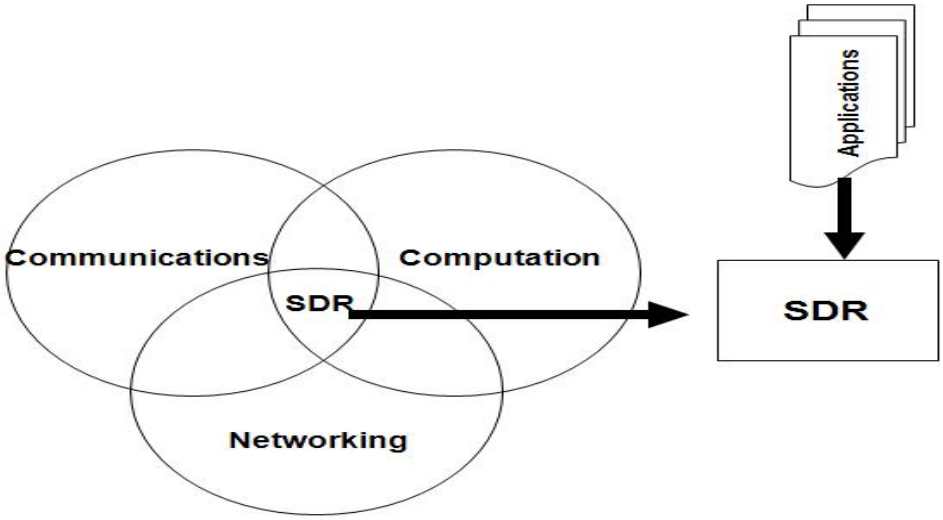


Figure 1.1 Common part is SDR among three major streams.

Basically, the common part of communications, computation and networking is SDR (Seung and Yu, 2002) as shown in Figure 1.1. The goal of a SDR is to move as much of the processing in the radio from fixed hardware to software (Bing, 2005), with the intention of making the function of the radio more configurable. Ideally, a software-defined radio consists of an ADC connected to an antenna (Manteghi, 2003). The digital output is fed into a configurable computation device for processing. In practice, however, an analog front-end (Puvaneswari, 2004) is necessary. RF processing and down conversion (Andersson et al, Nov. 2006) are performed in the

analog domain before the ADCs. SDR (Nakajima et al, 2001) is evolving towards the ideal. Future SDR might replace fixed analog hardware with an intelligent software-controlled RF front-end (Laddomada et al, 2001). The operation of the radio can be today's exceedingly rapid pace of technological (Chapin and Sicker, 2006) advances make communication devices become obsolete shortly after they are produced.

1.2 System Architecture of the Software Defined Radio

The schematic diagram of the SDR is shown in Figure 1.2. It consists of RF, IF, and base band. The SDR architecture consists of several parts as shown in Figure 1.3. The design begins with the antenna. Wideband antennas and interference mitigation are needed. The second part is the RF frequency unit, which is similar to a hyper heterodyne receiver, but not identical. The digital circuits are also important. The ADC, DAC, DSP, etc. units must be designed or selected carefully. Finally, the software design must be on an object-oriented approach. In first approach as shown in Figure 1.3 the RF and local oscillator (LO) signals (Rykaczewski et al, 2005) are mixed directly and the resulting analog signal is converted to the digital regime. In this case, the DSP does the main functions namely, the demodulation, the clock recovery and the symbol reception. The problem is that this approach can insure only slow speed (few kbit/sec) (Hogari et al, 2008), because the DSP has a lot of tasks and it has not enough capability for it. This problem can be overcome with a special chip, namely programmable down-converter (PDC) which covers the down conversion (Tseng and Chou, 2006), digital filtering (Johansson and Wanhammar, 2000) and decimation. This device uses a numerically controlled oscillator (NCO) to produce the sinusoidal signals, which are necessary for the conversion to baseband. So the DSP works on a slower speed and realizes only the demodulation, clock recovery and configuration of filters (Mahesh and Vinod, 2008). This concept enables higher data transmission velocity (several Mbit/sec). In this case, the DSP gets only the converted information signal. This is the direct conversion solution.

Phase mismatch occurs when phase difference between local oscillator signal for the in-phase and quadrature (I and Q) channels is different from 90 degrees. The gain mismatch between I and Q channels results from channel components gain mismatch.

The end result of IQ imbalance in a quadrature receiver is the frequency interference aliasing into the desired signal band which reduces the dynamic range and degrades the receiver performance.

The main components of interest in this are the duplexer or circulator and RF power amplifiers. The duplexer may take the form of a simple switch (Gabor et al, 2006), which has advantages including wide bandwidth. However, there may be issues with isolation, and the transmitter may need to be disabled to avoid saturating the receiver in receive mode. If this is the case, the transceiver cannot transmit and receive simultaneously which would be a significant limitation. The use of a circulator would allow simultaneous transmit and receive operations, but these devices generally have narrow bandwidth and poor isolation. They are generally used to isolate the antenna (Marrocco et al, 2006, Marrocco and Mattioni, 2006) from the transmitter to relax the specification on antenna input match. Considerable research has been conducted into the linearisation of power amplifiers and a number of techniques exists and are widely employed. For narrowband systems, typical intermodulation product levels of -70 dBc can be achieved with conventional techniques. If this is to be extended across a broader band, more sophisticated pre-distortion and feedforward techniques need to be applied. Numerous receiver architectures may be employed to deal with these various issues.

It is alarming, but perhaps understandable, that antenna technologies for SDR applications have not been widely examined. They do not generally appear as a separate block in the 'system design' as most RF systems are relatively narrow band. RF system designers are broadly more concerned with antenna gain/directivity, radiating characteristics, input match characteristics or voltage standing wave ratio (VSWR) and cross-polar rejection. Of course, this is a sweeping generalisation, but many applications require bandwidths that are readily achievable using existing antenna designs.

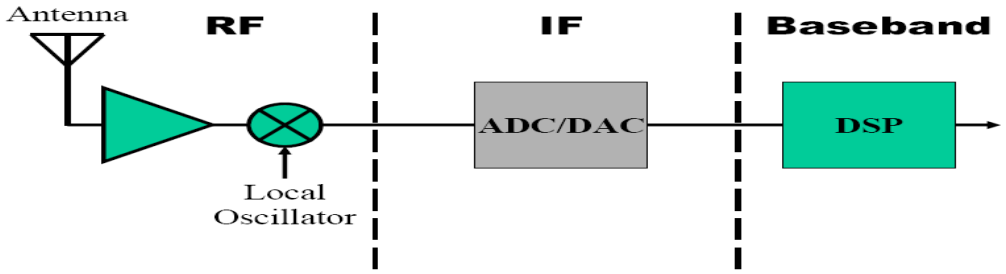


Figure 1.2 Schematic of the SDR.

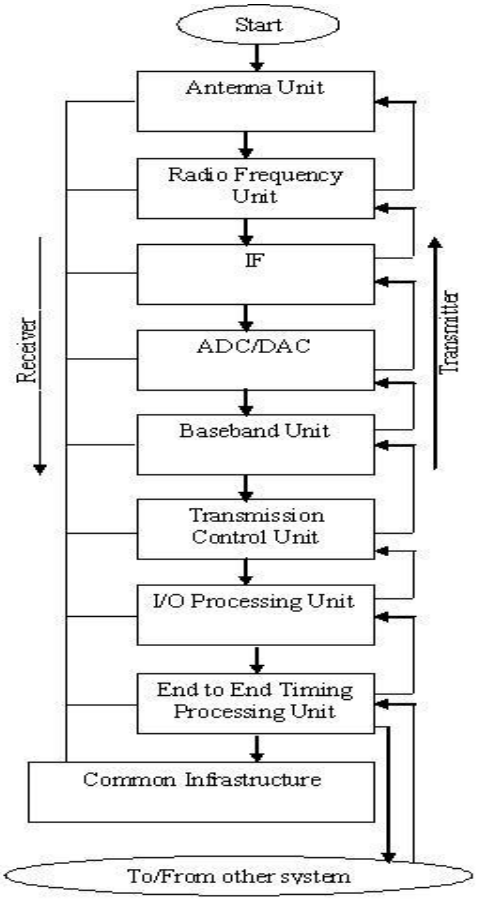


Figure 1.3 Commonly used SDR receiver/transmitter.

This architecture implements channel coding, source coding and control functionality in software on DSP/ programmable logic. It allows a measure of new service introduction onto the phone in the field; in effect it allows reconfiguration at

the very top of the protocol stack (Emmons and Chandler, 1983), the applications layer (Chun et al, 2004, Lewan and Long, 1983). Baseband modem (Burger and Huang, 2001, Van and Collados, 2007) functionality is implemented in software, which allows the realization of new and adaptive modulation schemes under either self-adaptive or download control. Intermediate frequency (IF) signal processing (Savoldi and Gubian, 2008) is implemented digitally in software, will allow a single terminal to adapt to multiple radios interface standards (Bing and Jayant, 2002) by software reconfigurability that is reconfigurability at the lowest level of the protocol (Kesller, 1988) stack. The software communications architecture (SCA) (Pucker and Holt, 2004) uses the common object request broker architecture (CORBA) (Lin et al, 1998) to allow an SCA-compliant radio system to perform its software processing across multiple processing elements. Although the SCA software is created to be run on general-purpose processors (Wong et al. 2000), the SCA acknowledges the use of FPGAs (Chee, 2003) and DSPs as part of the digital processing in an SCA-compliant radio. The military (Lackey and Upmal, 1995) needs smart radios that can flexibly work in whatever country they are deployed, since they may be interacting with local forces on different networks (Salwen et al, 1988). Cell phone makers need to consolidate the multimode radios they are building into their handsets and provide bug fixes with downloaded software. As a test platform for wireless communications (Shiba et al, 2002) researchers, an SDR allows for the testing of different modulation and demodulation schemes, multiple access protocols (Folts, 1979), and any other aspect of the radio processing that can be done in the digital domain. As a final product, an SDR is attractive to several groups:

- Wireless handset (Shiba et al, 2001) creators want to fix bugs more easily and to remotely re-flash devices.
- Military organizations are interested in interoperability, cost effectiveness, flexibility, and remote network management (Johnson, 2006).
- Civil government and public safety groups want access to new services and new frequencies.
- Radio vendors want reduced costs and increased flexibility.
- The federal communications commission (FCC) is interested in the possibility of SDR-enabled spectrum sharing.

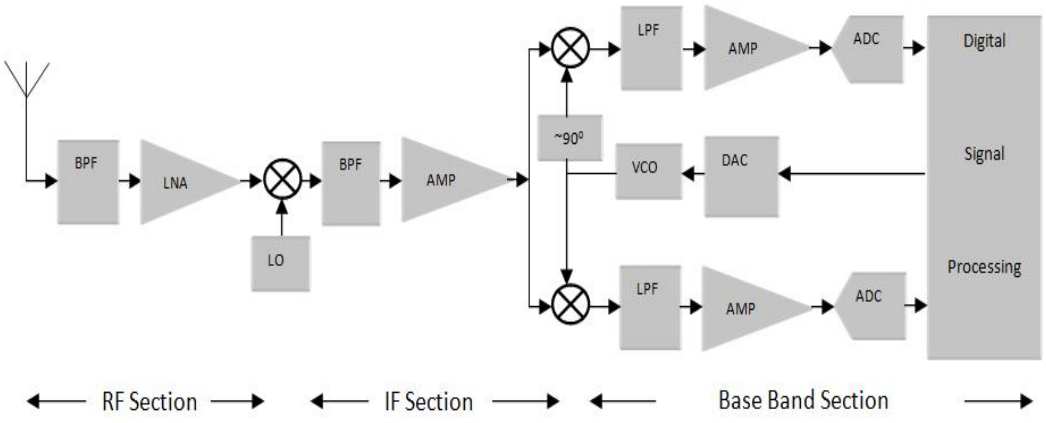
In order to achieve these goals, SDR technology (Sadiku and Akujuobi, 2004) needs to be further advanced to satisfy security, safety-critical, and footprint issues. The ultimate goal for software radio is to perform the ADC conversion directly at the antenna so that all signal processing (Kaur and Raj, 2008) could be done in software. The question of where one does the ADC conversion determines what radio functions can be moved into software and what types of hardware are required. For our purposes, we stake out a middle ground that we feel balances the need to capture what is really different and innovative about software radio with the limitations of current and near-future technology. Therefore, we consider it software radio if it involves ADC conversion at least the IF stage with the capability to support software processing thereafter. Whether subsequent stages are implemented in dedicated or general-purpose hardware is not critical to the definition of software radio, but certainly, the earlier ADC conversion and software implementation makes it more feasible to shift to general-purpose hardware. Two key technical limitations make it infeasible to do the ADC conversion at the antenna. First, digitization of the RF signal requires the incoming signal to be sampled, which results in the conversion of the waveform data into a sequence of numbers corresponding to each sample. The higher the frequency, the higher the required rate of sampling to accurately represent the signal. Additionally, the more information in the signal, the higher the resolution required to capture the information that is, the more bits that must be represented per sample. Taken together, this means that high bandwidth and high resolution, high frequency RF transmissions require very high sampling rates (Bose et al, 2008). The ability to support very high sampling rates, which is especially critical with the use of higher frequency signals, limits the range of what can be digitized. Indeed, it is only recently that sufficiently fast DSPs and wideband ADC chipsets have become available at affordable prices to make it feasible to contemplate ADC conversion of the IF rather than the baseband signal. Second, it is difficult to design linear amplifiers that can amplify the wideband signal at the antenna without distortion. Linear amplification is needed to keep the signal from being lost in the noise that accompanies the signal received at the antenna. Although new amplifier designs and

pre- and post-amp signal processing techniques can alleviate some of these difficulties, employing these increases the cost of the radio.

We expect the software radio to evolve such that the point of digital conversion moves closer to the antenna, and antennas become able to receive a wider swath of the useable RF spectrum. This will increase the spectrum agility of future radio designs, as digitization shifts from baseband to IF it is possible with today's emerging generation (Wiesler and Jondral, 2002) of software radios to the goal of RF digitization at the antenna. Concurrently, we expect to see a shift from the current generation of dedicated hardware embodied in application specific integrated chip (ASIC) (Vogt and Wehn, 2008, Li Min et al, 2008) to programmable ASICs, then to DSPs, and finally, to more general-purpose computing platforms such as PDA (Feng et al, 2003) or PC CPUs. Figure 1.4(a) shows a typical super-heterodyne radio receiver, in which the signal passes through many analog components for example amplifiers filters (Koochakzadeh et al, 2008) and mixture that have non-ideal performance and are subject to influence such as temperature differences and humidity. Therefore, the signals accumulate many distortion along its processing path. An ideal receiver should be capable of receiving and transmitting RF signals, interoperability many given air interface radio standard using software. In order to do so, the ADC should be shifted as close as possible to the receiver's antenna as shown in Figure 1.4 (b) compared to the traditional super-heterodyne receiver, the ideal SDR receiver contain minimal quantity of analog components. Earlier, conversion of the RF signal to digital not only allow more flexibility in signal processing but also provide higher signal fidelity as analogue components do not perform ideally and might significantly alter the behavior due to external influence that is temperature, humidity etc. Other advantage of digital component is small footprints, low power, consumption and fast development (time to market).

However, some key issue still prevents the realization of an ideal SDR receiver. Antenna that ideally receives and transmits wideband of frequency is not realizable with currently available technology. Suppose the antenna problem is overcome, another problem stems from the ADC bottleneck. According to the Nyquist – Shannon sampling theorem, a periodic signal should be sampled in rate which is at least twice its frequency in order to be able to reconstruct it. A 2 Giga sample per

second (GSPS) ADC could therefore sample periodic signal upto 1 GHz of frequency. Other fundamental limitation of ADC due to its non-ideal nature are low resolution (quantization error), non-linear behavior, deviation from accurate sample timing intervals (jitter error) and noise, which limits its performance (Hentschel et al, 1999). Third inherent problem in the ideal SDR results from the limit of now a days computational power. Assuming that a perfect ADC exists, the amount of digital information (samples) to be processed by the digital signal processing unit surpasses the computational capacity of presently available computing platforms and might requires giga floating point per second (giga-FLOPS) performance. The limitations discussed above lead to the conclusion that a compromise should be devised in order facilitate the implementation of SDR receiver. Figure 1.4 (c) depicts possible architecture for feasible SDR receiver. Limiting the bandwidth of the receiver makes it possible to device a suitable antenna and alternative ADC sampling rate limitation and computational load. Therefore, IF stage is introduced in order to deal with ADC bandwidth limitations. Furthermore, a digital front-end (Vun and Premkumar, 2005) stage is appended in front-end of DSP platform can take over computationally intensive tasks from the software driven platform. These tasks may include sample rate conversion, pulse-shaping, digital beam-forming (Singh et al, 2006), frequency allocation and other tasks derived from the receiver's target applications. The digital front-end is likely to be implemented in firmware field-programmable gate array (FPGA) (Medany, 2008, Noseworthy and Leeser, 2008) and flexible ASIC digitizers, which provides a trade-off between performance and flexibility.



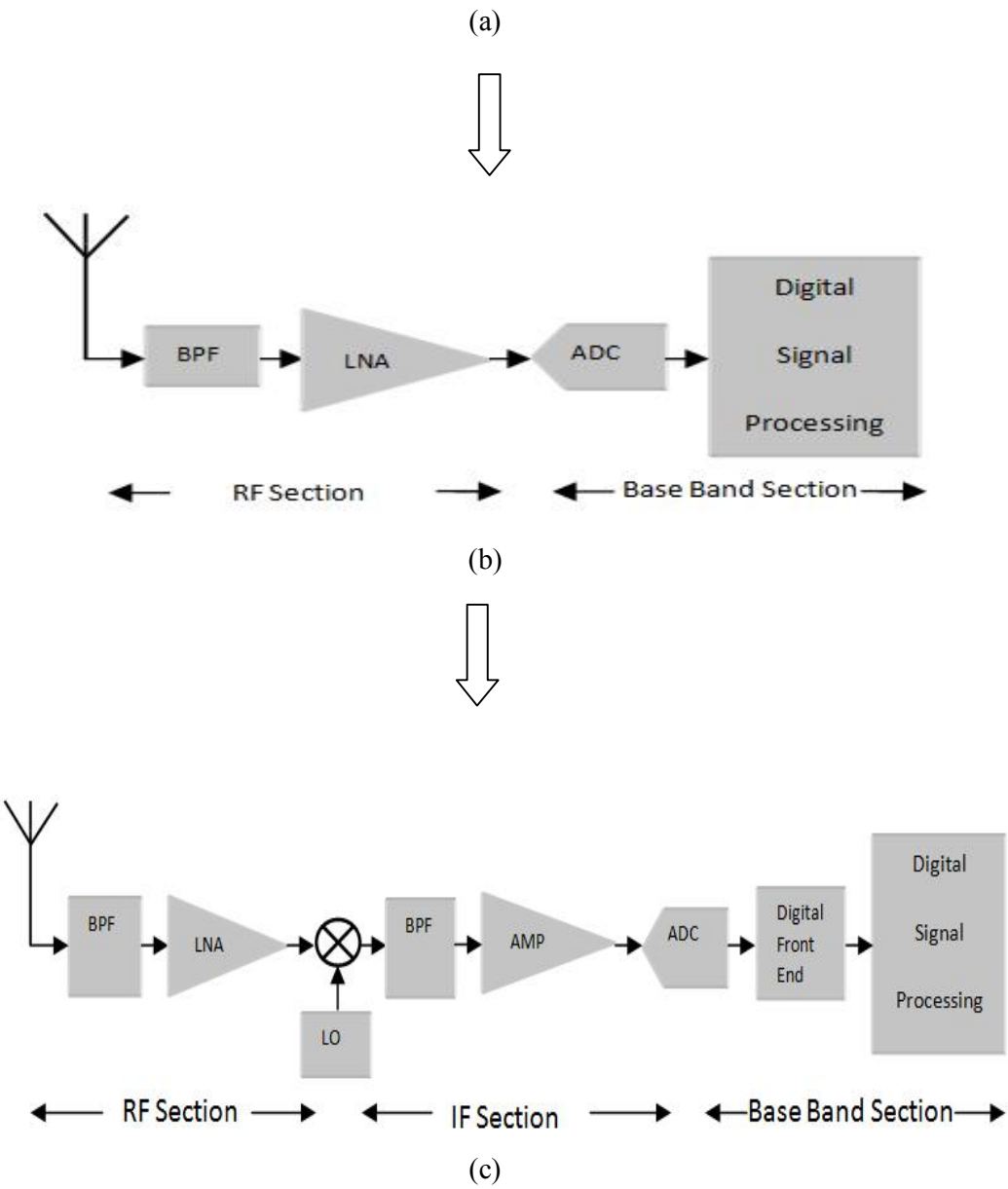


Figure 1.4 (a) Superheterodyne (b) Ideal and (c) Feasible SDR.

An ideal software radio does not have any analog stages for signal processing, except antenna, power amplifier and microphone or loudspeaker. In this case, the analog signals in the receiver are converted to digital virtually right next to the antenna. These signals can then be handled by the necessary processor. As the name

"ideal software radio" implies, this device is not yet feasible at least not with today's technology. However, SDR are feasible as shown in Figure 1.4 (c).

SDR components can be divided into analog and digital as shown in Figure 1.4. Even in the age of digital technology, the analog components in SDR such as antennas, band pass filter and low noise amplifier (LNA) play a critical role and determine a radio's performance properties. Analog to digital conversion is right after the RF parts in order to digitally elaborate the signals on a programmable board. The flexibility of the terminal to adapt to different standards and protocols is implemented by using reconfigurable and reprogrammable hardware in a DSP board. Some other functions can also be implemented by programming in the digital domain. However as we mentioned above, it is just the idea architecture, which means it not feasible to use one single RF stage for a multi-mode, multi-bandwidth system since it is impossible to build an antenna or LNA on such a wide bandwidth ranging from hundreds megahertz to tens gigahertz. Also, in this case, the requirements for ADC is too stringent to be implemented (Puvaneswari, 2004).

The ability to process wide band frequencies is quite import characteristic for multi-band system design. In order to overcome this bottleneck, several receiver architectures are proposed and widely used in different situations. An important concept, intermediate frequency (IF) was proposed by researchers. An IF is a frequency to which a carrier frequency is shifted as an intermediate step in transmission or reception. It is the beat frequency between the signal and the local oscillator in a radio detection system. As one stage in many types of receivers, the IF stage shifts the radio frequency to a selected intermediate frequency. There may be several such stages in one radio receiver. By using the IF stages, the stringent requirements for ADC are dramatically reduced. Also the antenna and LNA are much easier to satisfy the general demands from the whole system.

One conventional radio receiver architecture, named, superheterodyne is widely utilized in most RF communication transceivers manufacture today. This architecture has existed for almost one century and was proposed by Edwin H. Armstrong in the 1910s. Normally in the literature there are 'heterodyne' and 'superheterodyne' architectures which are not discussed very often. To 'heterodyne' means to mix to frequencies and generate a new frequency by either the sum or the difference of these

two original frequencies. However to 'superheterodyne' means only produce the new frequency by selecting the difference of two original frequencies.

In order to choose a suitable IF, many kinds of interferers should be taken into consideration. Compared to intermodulation, Image problem is the most serious challenge for IF selection. According to the discussion above, we can draw the basic rules for IF selection. The IF receivers down convert the RF signal to an intermediate frequency by the local oscillator. There are two types of IF receivers, Low-IF receivers where the IF could be either one or two times the information bandwidth and wideband (Singh et al, 2010) IF receivers in which the IF can be selected arbitrarily depending on the system requirements and communication demands. IF-receivers combine the advantages of both presents the Low-IF receiver architecture. As it can be seen, one IF stage follows the RF stage (Brock et al, 2001) and the signal is digitalized directly by ADC converter after being converted to a low IF signal. There is no direct current (DC)-offset problem in Low-IF receiver compared to homodyne receivers because the signal is converted to a bandpass signal with a center frequency of one or two times the information bandwidth other than DC. Also, due to the simple architecture, Low-IF receivers have high level of integration. However, because of the low IF, the image band is so close to the information band and it is hard to reject the image signal using the RF Bandpass filter. ADC converters will sample both the image and desired signal simultaneously. The further down conversion form low IF to baseband is realized in the digital domain without having the problem of I/Q mismatch existing in analog domain.

This receiver takes all of the channels (Costa and Haykin, 2008) and frequency translates them from radio frequency to intermediate frequency by multiplying the output of the LO with a fixed frequency. The low pass filter (LPF) following the mixer is used to remove the frequency components above the IF band. All the channels at IF are then translated to baseband with a tunable channel-select frequency synthesizer. Afterwards, the selected lowpass channel signal is converted to digital signal by an ADC converter.

The choice of IF depends on trade-offs among three parameters: the amount of image noise, the spacing between the desired band and the image, and the insertion loss of the image-reject filters. In order to minimize the image, we can either increase

the IF or tolerate greater loss in the filter while increasing its Q. Since the gain of the LNA is typically less than 15dB, the filter loss should not exceed a few dB, reducing the trade-off to a choice between the image noise (Kwon et al, 2007) and the value of IF. From the above discussion, we know that the choice of IF influences the trade-off between the image rejection and channel-selection. Because the image corrupts the sensitivity of the receiver, we can say the choice of IF entails a trade-off between sensitivity and selectivity. In the following paragraphs, several problems should be taken into consideration when we are doing the IF selection.

The three main methods of transceiver architectures are sampling the first IF signal, direct conversion and direct RF sampling. Every method has several advantages and disadvantages. In our system the direct conversion was chosen and realized. It means a receiver with zero IF (intermediate frequency). Its main advantages are: only a lowpass filter is required which is easier to implement; flexible there is no image frequency and only one LO noise contribution is encountered. However there are difficulties as well. The first is the spurious LO leakage from the receiver (Studenberg, 2007) into the antenna generating an in-band interference. Another problem is the dc offset in the receiver. The LO signal is leaking to the antenna, then reflecting and self-downconverting to DC. On the other hand there is a large near-channel interference leaking into the LO port of the mixer, then self-downconverting to dc. These problems can be reduced by shielding and good circuit design. The digital IF sampling and down-conversion would need high performance analog to digital converter which is flexible but expensive and has little dynamic range. Presently, 12 bit 30 MHz ADC converters are commercially available. The operation frequency range tends toward the higher microwave regions. Therefore good synthesizers (for the transmitters) and low phase noise, tunable, small size and wide operation range microwave local oscillators for the receivers are needed. The traffic (Manfield et al, 1993) demands should be followed as flexibly as possible. As the bit rate of the transmitted information is changed the transmission bandwidth is also varied. In case of different data rates the bandwidth has to be flexible at the same signal-to-noise ratio. This problem can be solved by conventional hardware approach a tunable filter with yttrium iron garnet (YIG) sphere or switching of fix tuned filters. In our case the filters are realized in a software way.

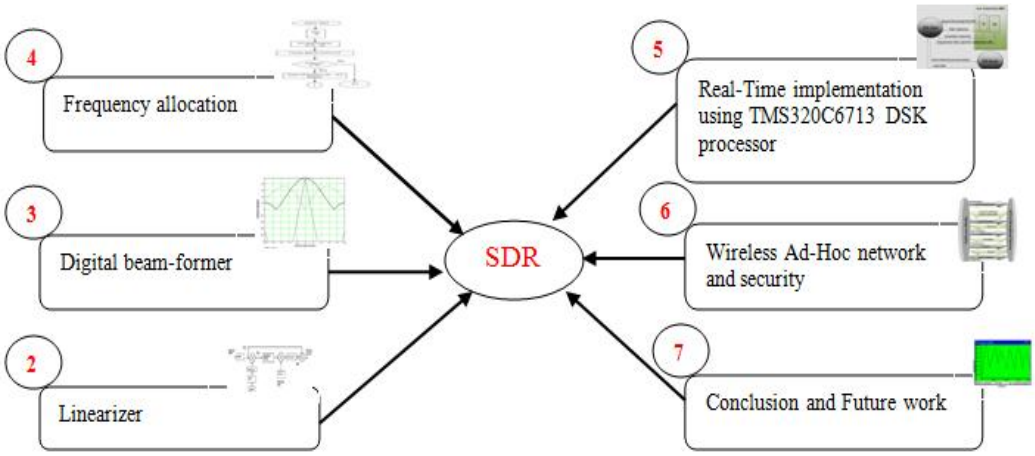


Figure 1.5 Overview of the thesis.

1.3 Organization of the Thesis

The major challenges in SDR are pulse shaping, digital beamforming, frequency allocation, communication, security and reconfigurability. This thesis covers different topics related to the SDR, from the problem statement to the implementation. The main body of this thesis is schematically depicted in Figure 1.5.

In Chapter 2, we present the problem associated to nonlinear behavior of the pulse. A problem is presented in literature, but still open since it has to continuously handle with new communication scenarios where linear amplification is must. Here, we have chosen Rayleigh first order and then we have linearized it. After amplification linearity is lost, so we have overcome this problem.

Chapter 3 provides a digital beam-former with low angle resolution. Here we have used array of antennae to solve our problem of SDR. Here we have used the concept of SUM-3Difference in order to accomplish our problem. Most of the concept used from computer system organization e.g. digitization, D flip-flop etc.

Chapter 4 presents an overview of frequency allocation in SDR so that it can be switched to local available frequency by service provider in order to avoid limitation of bandwidth of defined spectrum. In this chapter a new idea is proposed to implement this using DBMS and SD Micro Card.

Chapter 5 is all about Real-Time Implementation of Program using TMS320C6713DSK Processor. Here we have configured multichannel buffered serial

port (McBSP) first by using code composer written in C language. We made our own hardware and interfaced it with DSP Kit and CRO to see the output. We got the output even by four times overlapping obviously by maintaining Nyquist criterion.

In Chapter 6 we aimed at validating the functioning of Wireless Ad-Hoc Network with SDR. In this chapter a novel approach is used in context with Ad –Hoc network. The parameters of communication in ad-hoc networks changes such as the distance between nodes channel characteristics, and person who is using it changes frequently. We can change software specification rather than changing any hardware Such as chip every time. Change of hardware leads to wastage of money. In this way SDR is economically beneficial to us. Here we are using concept of M-ary phase shift keying (MPSK) technique for adaptive detection. By using MPSK we find that MPSK signal can use two carrier signals that are perpendicular to each other for coherent detection. So it can be used for military purpose also.

Finally, Chapter 7 concludes the thesis and proposes possible future lines of research.

CHAPTER-2

LINEARIZER FOR PULSE-SHAPING OF RECEIVED PULSE

2.1 Introduction

In this chapter, we have considered the radio frequency (RF) linearization for an efficient operation of the SDR. The power amplifier is a key element in every radio communications (Tarver et al, 2001) system, and is required to serve the function of amplifying the information-bearing signal, without distortion, in an efficient manner. However, distortion in power amplifiers occurs in two different ways:

- Nonlinear distortions
- Linear, temporal and frequency dispersive effects.

Nonlinear distortions arise from the fact that a power efficient conversion of supplied DC power to RF signal power requires a nonlinear operation of the amplifier to a greater or lesser degree. Employing nonlinear amplification reduces the signal fidelity, so-called 'in-band' distortion occurs, due to the generated harmonics, out-of-band emissions occur, which can potentially cause interference to users in neighboring frequency bands that is another drawback of non linear amplification. Due to nonlinear effects, energy is transferred into undesired bands, thus lowering energy efficiency also linear, temporal and frequency dispersive effects. Dispersive effects in power amplifiers are caused by internal memory effects. In the narrowband systems dispersive effects typically can be neglected. However, in wideband systems, the effects of dispersion can be significant. Whilst analogue linearization methods exist, they are unable to compensate fully for linear dispersion effects. However, digital pre-distortion techniques are able to counteract the effects of both nonlinearity and linear dispersion.

The dispersive effects in power amplifiers have their origin in internal memory effects. Memory effects with long time constants that is, in the order of one second occur due to thermal and trapping effects causing linear time dispersions. Memory effects with short time constants occur due to non-vanishing transit times in

transistors as well as the analogue circuitry, bonding inductances, capacitances and resistances causing linear frequency dispersion of the signals. In order to observe the dispersive effects, certain signal properties are required. If the symbol period of the signal is small compared to the inverse of the bandwidth that is to be transmitted by the power amplifier, the dispersion effects can be neglected. Nonlinear effects, however, become visible even for small signal bandwidths. The presence of both linear dispersive and nonlinear memory less effects shows up in some unpredicted way, most modern wireless systems employ linear modulation schemes. Therefore, linear behavior at the output of the power amplifier in any 'generic' SDR platform is essential. Furthermore, as signal bandwidths increase, measures to compensate for linear dispersive effects will also be a requirement. This is especially true in the case of generic platforms when it will not be possible to optimize the RF front-end for any one particular radio system. Luckily, the inherent flexibility of SDRs makes them well suited to the implementation of advanced, adaptive pre-distortion algorithms in the digital domain. Linearization methods incorporating both static and dynamic amplifier models have been discussed. In addition, simulation results that clearly show the performance to be gained by implementing such techniques have been presented.

In this chapter, we present a novel concept of pulse-shaping in an ultra-wideband (Porcino and Hirt, 2003) radar system. Instead of attempting to design an antenna with flat group delay, the emphasis has been shifted to the signal processing aspect of pulse-shaping (Tan and Beaulieu, 2004). The received pulse which has broadened due to dispersive phase response of the propagating channel is shaped back closer to the ideal pulse using a linearizer (Kenington, 2002). The block schematic of the linearizer is presented along with simulated results. Though only Rayleigh first order pulse has been used for simulation purpose, the method can easily be generalized to incorporate other pulse shapes. After recognizing the potential advantages of the ultra-wideband (UWB) (Choi et al, 2003), in 2002 the Federal Communications Commission (FCC) allotted the band of spectrum from 3.1 GHz to 10.6 GHz for unlicensed use for communications and imaging technology. A UWB definition was created as a signal with a fractional bandwidth greater than twenty percent or which occupies more than 500 MHz of spectrum. For communication applications, high data rates (Srikanteswara et al, 2001) are possible due to the large number of pulses that can be

created in short time duration. The UWB technology is popular for its multipath immunity, high data throughput, better wall penetration, low power consumption, and low probability of interception and detection. Because of all these interesting features UWB technology has become increasingly accepted for numerous applications in civilian and military field.

Chen et al (2004) have presented two vital design considerations in ultra-wideband radio systems, the radiated power density spectrum shaping with certain emission limit mask for coexistence with other electronic systems and design of source pulses and transmitting / receiving antennas for optimal performance of overall systems. A frequency dependent transmission equation based on the Frii's transmission formula is employed to describe transmitting / receiving antenna systems. Then the selection of source pulses is done with emission control consideration. The received pulses are studied using both narrowband and wideband antenna system. Cramer et al (2002) describes the results of an ultra-wideband propagation study in which arrays of propagation measurements are made. An approach to the spatial and temporal decomposition of an array of measurements into wave front impinging on the receiving array is presented. Ma and Jeng (2005) study the system transfer function for complete study of transmitting / receiving antenna system. In this chapter emphasis has been drawn on perfect design of UWB antennas which will show minimum distortion in the received pulses.

The antennas in UWB systems are pulse shaping filters. The transient behavior of antennas linear systems designed to process signals having instantaneous bandwidths can be described with equal validity in either the frequency domain or the time domain (Ross, 1968). The purpose of the above mentioned communication is to suggest a time domain criterion for the design of wideband radiating elements in place of the conventional frequency domain specifications, viz., a "flat" amplitude spectrum and "linear" phase function over a given band without specifications stipulated outside the band. In another significant work by Bennett and Ross (1978), researchers were introduced to the elements of time-domain electromagnetic, which includes base-band pulse technology and target-signature analysis. The solution of many problems of practical interest depends on estimation of the value $y(n)$ of a signal desired response by using a set of values from another related signal. Successful

estimation is possible if there is significant statistical dependence or correlation between the signals involved in the particular application (Manolakis and Ingle, 2005).

One may use a similar concept in the pulse-data transmission system where a copy of the transmitted pulse equalizes the received signal. The performance of data transmission system through channels (Schnepp et al, 2003) that can be approximated by linear system is limited by factors such as the finite bandwidth, inter-symbol interference (ISI), and thermal noise. When the channel frequency response deviates from the ideal of flat magnitude and linear phase, both tails of a transmitted pulse will interfere with neighboring pulses. If we know the characteristics of the channel, that is the magnitude response and phase response, we can design optimum transmitting and receiving filters that will maximize the signal-to noise ratio (SNR) and will result in zero ISI at the sampling instant. However, in practice we have to deal with the channels whose characteristics are either unknown or time varying. In this case, a receiver is designed that consists of a fixed filter and adjustable linear equalizer. In principle, to eliminate the ISI, we should design the equalizer so that the overall pulse shape satisfies Nyquist criterion (Deveugele et al, 2004):

$$\sum_{l=-\infty}^{\infty} H_r(F + \frac{1}{T_B}) = T_B$$

where we sample the received signal $x(t)$ at the time instant $t_0 + nT_B$. Normally the equalizer of choice uses digital finite impulse response (FIR) filters (Vinod and Lai, 2006). The goal of the equalizer is to determine the coefficients so as to minimize the ISI. Such equalizers may be zero-forcing equalizer (Lucky et al, 1968), or minimum mean-square-error (MSE) equalizer (Saltzberg, 1968).

In a new ultra wideband (Staderini, 2002, Han and Nguyen, 2002, Eldek et al, 2005, Eldek, 2006) ultra-short monocycle pulse generator is presented with reduced ringing. The step, Gaussian and monocycle pulses can be used in UWB systems. Among them, however, the monocycle pulse spectrum does not contain low frequency components. This attribute facilitates the design of components like antennas, amplifiers etc. In this chapter, such two-fold requirement is pushed to DSP in baseband. The transmitting pulse is used to equalize. Using neat but very simple

processing technique dispersion in the received pulse can be removed totally. The technique is outlined in the following sections as follows.

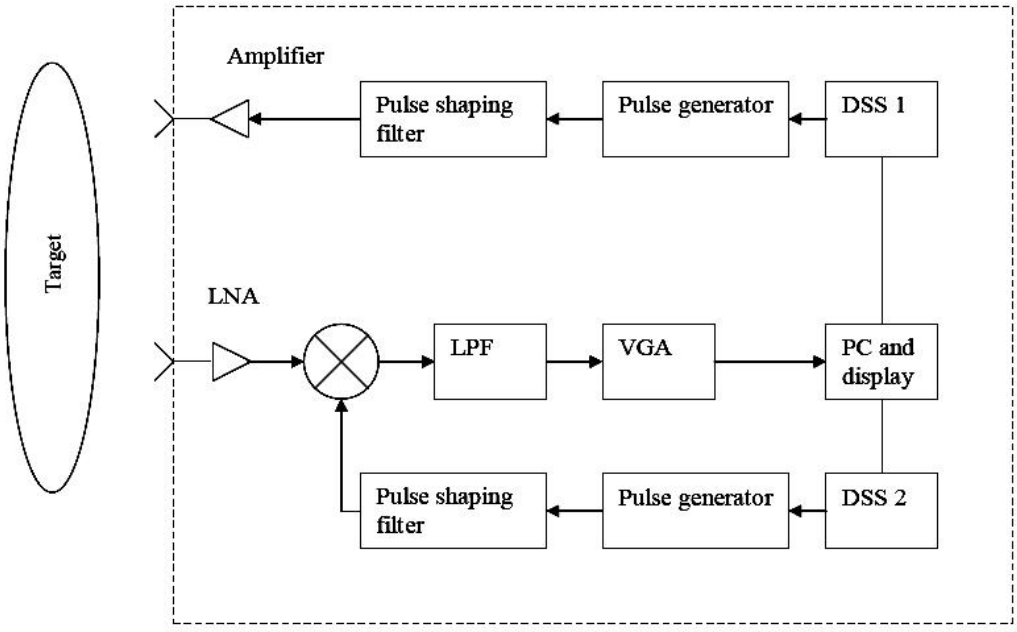


Figure 2.1 Schematic of typical radar transceiver of the SDR for monitoring target.

2.2 Schematic of the Transceiver

The schematic diagram of typical radar transceiver system architecture (Ivan and Narayan, 1999) is presented in Figure 2.1 the UWB radar is required to transmit sub-nanosecond pulses at discrete time interval which determines the pulse repetition rate. The UWB radar sensor consists of the three main sections: clock generator, pulse generator and transceiver. The direct digital synthesizer (DDS) is the clock generator. The clock generator consists of two direct digital synthesizers which are used to determine the pulse repetition frequency (PRF) of the sensor. The frequency and phase of the sensor can be adjusted through the DDSs. The output of the DDSs are passed through the pulse generator to create a fast rise time using step recovery diode which is further shaped by a pulse shaping filter. The transmit pulse magnitude is amplified to meet the FCC's ultra-wideband spectrum mask requirement. The signal processing (Alsliety and Aloi, Feb. 2007) unit consists of an integrator, digitizer and software algorithms to extract the desired information. Typically, to optimize the emission mask characteristics, PRF may also be random. The choice of PRF will

affect the emission mask, higher PRF will generate higher frequency tones. At the receiver (Schreier et al., 2001), more energy can be collected with the correlator. Since the position of the target is not fixed, the return UWB pulses will need to be synchronized with the reference signal at receiver (Abidi, May 2007). This is handled by the variable delay control within the DDS2 as shown in Figure 2.1. It send the reference signal at right time which is further to process by the pulse forming network (Baransel et al, 1995) to produce a short pulse at the local oscillator port of the mixer. The time delay control adapts to the position of the target. In the present proposal, the pulse shaping filter is removed from the receiver chain. A copy of the transmit pulse is used to correlate with the received pulse and simple algorithm is used to remove the effects of dispersion and is monitored on video graphics array (VGA).

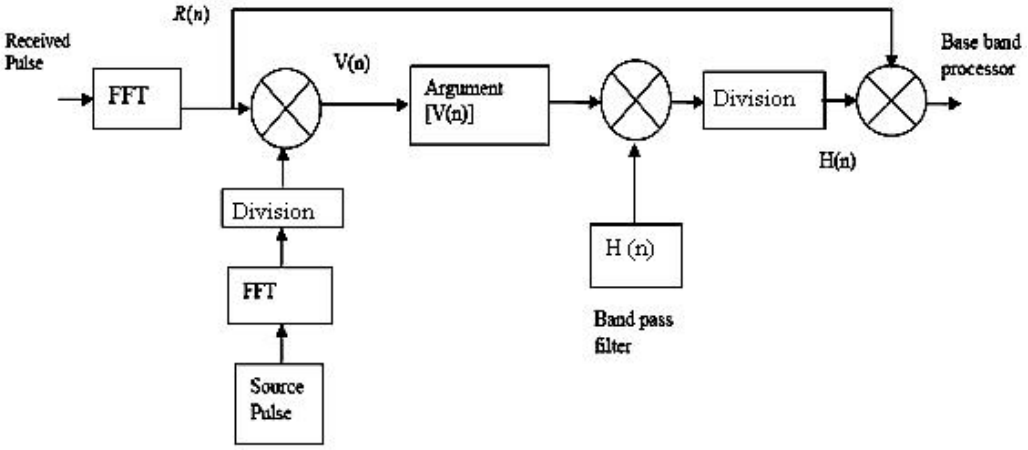


Figure 2.2 Block diagram of the proposed linearizer.

2.3 Concept of the Linearizer

The block diagram of the linearizer is presented in Figure 2.2 it is assumed that the received pulse is affected by the dispersive propagation medium. In the above schematic it is seen that copies of the frequency response of an ideal transmit used to linearizer the dispersive phase response of the received pulse. The incoming signal received by the antenna is digitized and converted into frequency domain. The frequency domain response of incoming signal is divided by the frequency response of the ideal transmit pulse and the phase angle of such is extracted as $V(n)$ which is then converted into a band pass response $H(n)$ with magnitude of unity. The original

signal $R(n)$ is then divided by $H(n)$ to get the received pulse with minimum pulse broadening. The band pass response is:

$$H(f) = \begin{cases} 1 & \text{for 3.1 GHz to 10.6 GHz} \\ 0 & \text{otherwise} \end{cases}$$

Mathematically, the complete operation can be explained as follows. Let us consider a single-input, single-output network where $x(t)$ is the input signal and $y(t)$ is the output signal. For a linear network with continuous-time variable x and y are related by a linear, integro-differential equation which may be Laplace-transformed, if there is no initially stored energy, to yield Y(s) = H(s) X(s). The quantities Y(s) and X(s) are respectively the Laplace transforms of $y(t)$ and $x(t)$, and H(s) is the network function. When $s = j\omega$, the network function is complex and may be written in the form

$$H(j\omega) = e^{-\gamma(j\omega)} \tag{2.1}$$

where

$$\gamma(j\omega) = \alpha(\omega) + j\beta(\omega) \tag{2.2}$$

Thus

$$\alpha(\omega) = -\ln H(j\omega)$$

and

$$\beta(\omega) = -\varphi(\omega)$$

The quantities γ, α, and β are all dimensionless, α being denoted as loss. Let us now consider the complete flow chart of the linearizing action. For explanation we consider only continuous time variable. Let x(t) be the ideal source pulse and r(t) be the received pulse. Then the transfer function $V(j\omega)$ can be given as:

$$V(j\omega) = \frac{R(j\omega)}{X(j\omega)} = \exp\{-(\alpha_1 - \alpha_2) - j(\beta_1 - \beta_2)\} \tag{2.3}$$

where for brevity ω argument is not reproduced every time. In this case α_1 and β_1 are the loss and phase component of the received pulse. In the next step we convert V(jω) as

$$V'(j\omega) = \exp\{-1 - j(\beta_1 - \beta_2)\} \tag{2.4}$$

In the final step the received pulse is extracted as

$$B(j\omega) = \frac{R(j\omega)}{V'(j\omega)} = \exp\{-(\alpha_1 - 1) - j\beta_2) \tag{2.5}$$

Therefore in the extracted pulse the dispersive phase component $\beta_1(\omega)$ is replaced thereby completing the linearizing action.

2.4 Results and Discussion

Due to unique temporal and spectral properties, a family of Rayleigh (differential Gaussian) pulses as defined is widely used as the source pulses in UWB system. The source pulse used in this configuration is first-order Rayleigh pulse $v(t)$ is given as $v(t) = \frac{d}{dt}[e^{-(t/\sigma)^2}]$ and the Fourier transform of $v(t)$ is $V(j\omega) = j\omega\sigma\sqrt{\pi}e^{-(\frac{\omega\sigma}{2})^2}$, (where we have taken σ = 200 ps). The received pulse is distorted due to dispersive phase response of the propagating channel. There is a group delay between the source pulse and the received pulse, because of the phase shift with respect to angular frequency. In Figure 2.3, a comparison of the ideal source pulse received pulse and the processed pulse is presented.

The frequency response of the received pulse is divided by the source pulse and the argument is extracted. This is converted to band-pass response using the relation: $H(n) = \cos\{\arg(v(n))\} + j\sin\{\arg(v(n))\}$. The original received pulse is then divided by $H(n)$. The result is plotted in Figure 2.3 from the Figure it is clear that the processed pulse-shape is closer to the ideal source pulse. However, since this method works with phase of the received pulse, the information content is not lost.

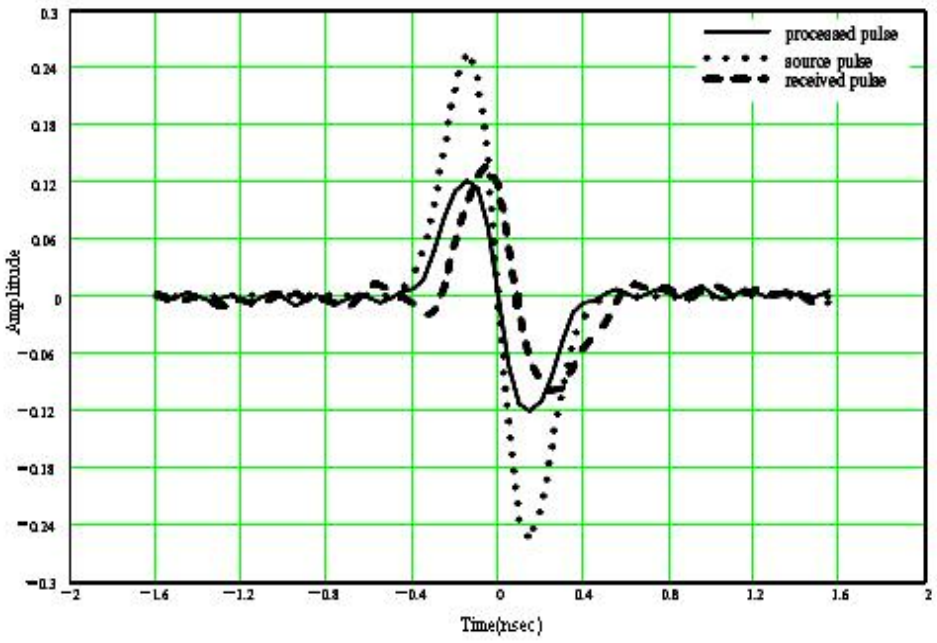


Figure 2.3 Comparative display of ideal pulse, received pulse and the processed pulse.

2.5 Conclusion

A novel schematic of utilization of DSP technique is presented which restores back the pulse shape distorted by dispersive propagation channel including the effect of spatial filtering done by the antenna. Using DSP a linearizing scheme is proposed.

The linearizing scheme is simple to implement using commercially available DSP processors. Simulation based results show promising outcome. With flexible radio architectures of the future comes the demand for high bandwidth signals. Since low-power power amplifiers are an indispensable part of the transmission chain, the demand for linearization methods is very high. When considering the high signal bandwidth requirement, only digital pre-distortion methods currently have the potential to supply such linearization. Due to their high bandwidth, power amplifiers show not only nonlinear but also dispersive effects that are difficult to handle in a general form. Thus adaptive algorithms are required with parameters and structure that can be changed depending on the current transmission (Dawoud, 2004) scheme. Further simulation/measurements on multi-path may be carried out to observe probable mitigation.

CHAPTER-3

A DIGITAL BEAMFORMER WITH LOW ANGLE RESOLUTION

3.1 Introduction

Recently, the SDR technologies are an attractive proposition for mobile communication systems. In particular, SDR systems have the potential to offer reconfigurable, multi-mode operation capabilities. A reconfigurable SDR provides the potential to upgrade or enhance the functionality of equipment without the need to change or modify the hardware.

A smart antenna (Perez-Neira et al, 2001) system seeks to add an additional degree of diversity to reduce interference between users and consequently increase user capacity through dynamic adaptation of the antenna's radiating properties. The most obvious example of this is a phased array antenna, an array of separate radiating 'elements' whose signals, when added together, form a beam. Flexibility and control over the beam shape is obtained during the beamforming process by altering the amplitude and phase of the individual element responses prior to summation.

In this chapter, we propose a digital beamformer for SDR by integrator method of detection. In the receive mode the digitized radar returns weights are allocate on the such a way that the first pulse reflect a SUM pattern and the subsequent three pulses reflect DIFFERENCE pattern. The pulses on DIFFERENCE pattern are added to each other and the net signal subtracted from signal received in SUM pattern. This results in very narrow beam which shows narrow spatial resolution. The schematic is presented and the results are shown. A beamformer forms one or more antenna beams anywhere within the arrays surveillance volume. Additionally, the beamformer adjusts the beam shape of the resulting beam with the aid of amplitude and phase weights associated with each antenna element (Fourikis, 2000). The array beam shape is defined by characteristics such as physical dimensions of array and amplitude/phase weights associated with each antenna element. Beamformers (Bond et al, 2003, Bindu et al, 2006) can have resistive network realization (Mills et al, 1963) or have transmission line realization (Fourikis, 1967). The Butler matrix has also been used in

many applications (Hall and Vetterlien, 1992). The Butler matrix consists of fixed phase shifts interconnected to hybrids and yields orthogonal beams. The lengths of the lines used are in units of $\pi/8$ radians and 180° hybrids are used.

Digital beamforming can be implemented when the arrays operate in transmit or receive mode. In radar context, digital beamformers (DBFs) are mainly used on receive arrays (Steyskal and Rose, 1989). DBFs have advantages such as fast adaptive null forming, the generation of several simultaneous beams, array self-calibration etc. In the radar system, detection is rarely done on a single pulse data (Skolnik, 2004). "*N*" pulses usually illuminate a target and returns are integrated coherently, before a target is detected (Lee and Kim, 2005, Choi et al, 2003, Fabbro, 2005, Seo et al, 2004). There are integrator types like moving-window integrator (Hansen, 1970), binary integrator (Harrington, 1955) etc. In these methods an effective value of SNR is obtained equal to SNR attributed to single pulse multiplied by *N*. The objective of this presentation is to utilize the radar technique of *N* pulse addition in digital beamforming method. It is shown that four consecutive pulses are digitized, stored and addition/subtraction operation carried out. It is shown that by the method followed, it is possible to create a very sharp beam which offers a spatial resolution much better than the conventional $\lambda/2D$, where *D* is the aperture dimension.

3.2 Generation of Sum and Difference Patterns

Consider an array of an even number of elements $2M$ is positioned in the *X*-*Y* plane with *Z* axis being the direction of propagation. The inter-element spacing is *d* and *M* elements are placed on each side of origin. Assuming that the amplitude excitation is symmetrical about the origin, the normalized array factor for SUM pattern (for non-uniform amplitude and same phase in each element) is given as:

$$(AFS)_{2M} = \frac{1}{M}\sum_{n=1}^{M} a_n \cos[\frac{(2n-1)}{2} kd \cos(\frac{\pi}{2} - \theta)] \tag{3.1}$$

where θ is measured from broadside direction. In the DIFFERENCE pattern, one half of the array has phase value of zero and the other half has phase value of π. The resultant array factor for DIFFERENCE pattern is:

$$(AFD)_{2M} = \frac{1}{M}\sum_{n=1}^{M} a_n \sin[\frac{(2n-1)}{2} kd \cos(\frac{\pi}{2} - \theta)] \tag{3.2}$$

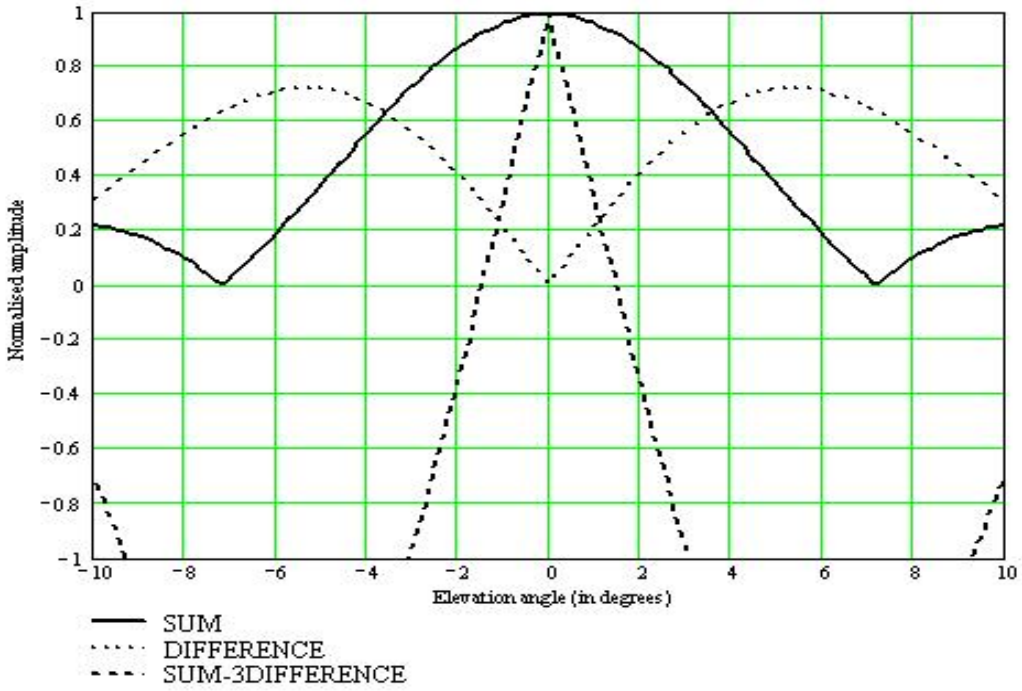


Figure 3.1 Display of SUM, DIFFERENCE and SUM- 3×DIFFERENCE patterns for uniform illumination.

We obtain SUM-3×DIFFERENCE pattern from subtracting three times equation (3.2) from (3.1). In Figure 3.1 the SUM, DIFFERENCE and the SUM-3×DIFFERENCE patterns are plotted. It is clearly seen that the beam width narrows for SUM-3×DIFFERENCE pattern. It is also generates negative amplitude over a large range of elevation angles. By controlling the progressive phase difference between the elements, all the three beams can be squinted to give a maximum radiation in a given direction (Alfred et al, 2006, Balanis, 2004). The numerical values of 3dB beamwidth with null depth are presented in Table 1. For such computation, we have considered eight elements only with spacing. The conventional beamwidth is $\lambda/2D$, where D is the dimension of the array. From Table 1, it is seen that even for imperfect null depth the resultant beamwidth does not vary significantly. For application in vehicle tracking radar, let us consider the SUM pattern only illuminating a moving vehicle at a distance of 30m. The radar's footprint will be 9m, whereas for the proposed case the footprint will be 1.6 m, therefore the proposed radar will be able to resolve to moving targets nearby each other. For example, if 10

ns is considered the pulse width, the interpulse period is 50 ns then the range resolution should be the order of 1.5m and maximum detectable range is 75 m. The target for four pulse integration will be 200 ns.

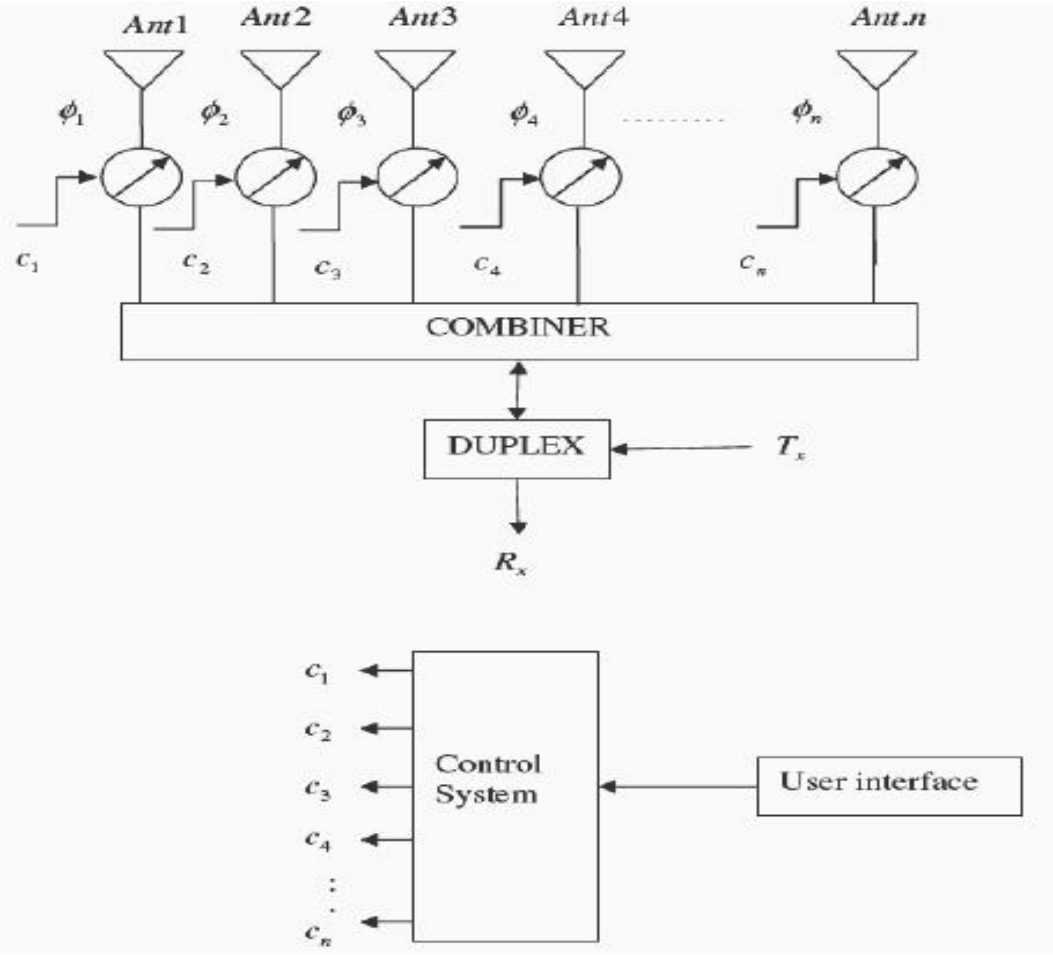


Figure 3.2 Schematic of the generation of the SUM and DIFFERENCE pattern in real time.

Considering highest speed of vehicle is 120 km/h, the vehicle will move 6.66 m, which is insignificant. When the radar is operating, microcontroller system controls the *c*1, *c*2, *c*3 . . . . . *cn* phase shifters and these signals *c*1, *c*2, *c*3 . . . . . *cn* controls the phase shift of each antenna as shown in Figure 3.2. For SUM pattern the phase differences $\varphi 1$, $\varphi 2$, $\varphi 3$ . . . . . φn are zeros and for the DIFFERENCE pattern the phase difference for one half elements is zero and for the rest half elements is π. So this is operation in real time.

Table 3.1 Beamwidth with null depth.

Null depth (in dB)	Beamwidth (degree)
-20	2.84
-18	3.20
-16	3.21
-14	3.21
-12	3.21
-10	3.21

3.3 Results and Discussion

The schematic diagram of proposed digital beamformer is shown in Figure 3.3. In this schematic, the received analog signal is digitized using analog to digital converter and the digitized data is then shifted using '*D*' type flip-flops after each pulse duration. After receiving four consecutive pulses, the addition of second, third and fourth pulse is subtracted from the first pulse using parallel adder and parallel substractor, respectively. The corresponding timing diagram is shown in Figure 3.4. The pulse is transmitted from the radar and received after time τ . *Ts* is the inter pulse period of transmitting pulses, so after each *Ts* the pulses are received. The time moments, at which we receive the first four pulses are τ, $\tau + Ts$, $\tau + 2Ts$, $\tau + 3Ts$, between two consecutive pulses we have large number of range gates. So it is difficult to implement it by using thousands of flip-flops. Hence, we have proposed to use array concept for storing these ranges. Consider the first received pulse is SUM and consecutive three pulses are DIFFERENCE. Five single dimensional arrays are taken named Arr1, Arr2, Arr3, Arr4, ResArr. We are storing these large number of range gate values in Arr4, Arr3, Arr2 and Arr1, respectively. The result of SUM-3×DIFFERENCE that is, Arr1-(Arr2+Arr3+Arr4) is stored in ResArr, hence it reduces the complexity of using thousands of flip flops. Before taking the new values, all the arrays are reset to zero. This logic is shown with the help of flow chart in Figure 3.5 with null depth.

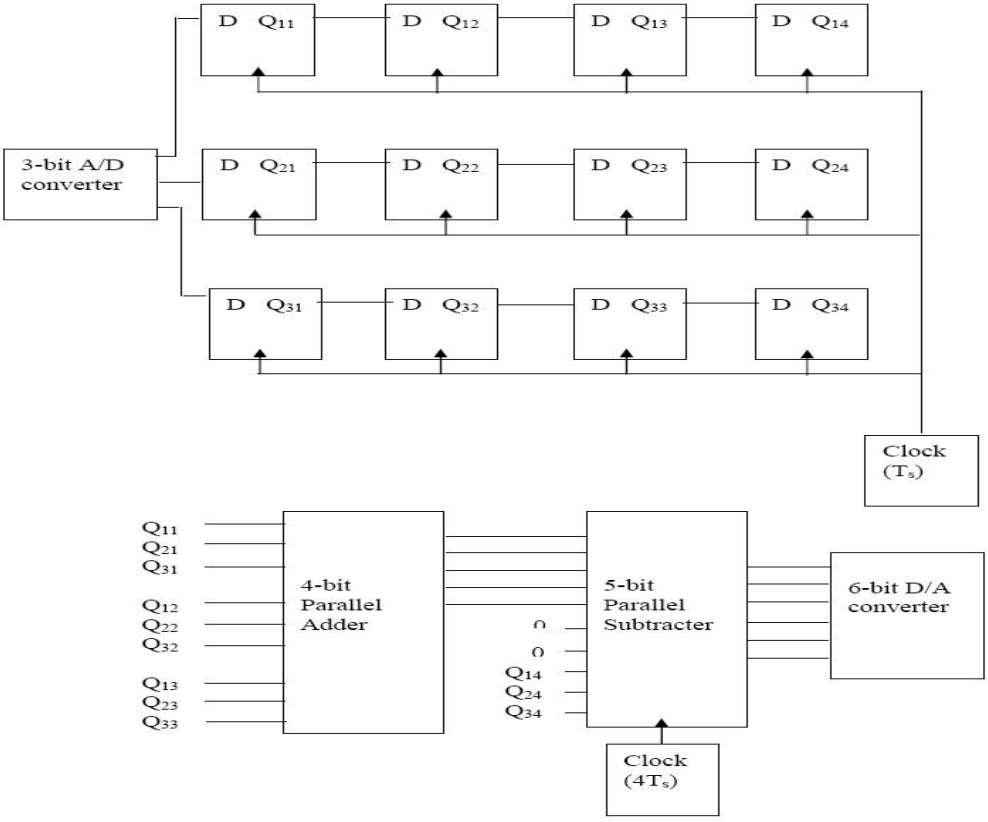


Figure 3.3 Schematic diagram of the digital beamformer.

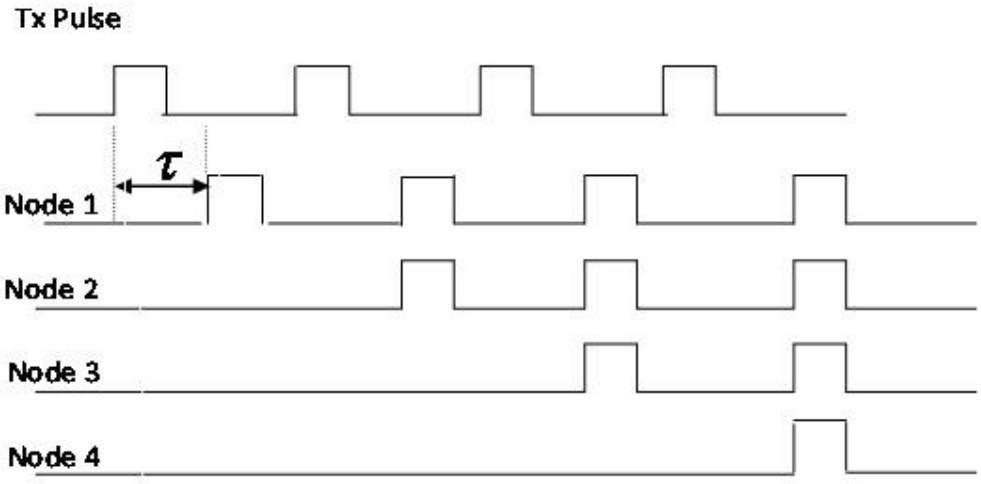


Figure 3.4 Timing diagram with respect to the transmitting pulse.

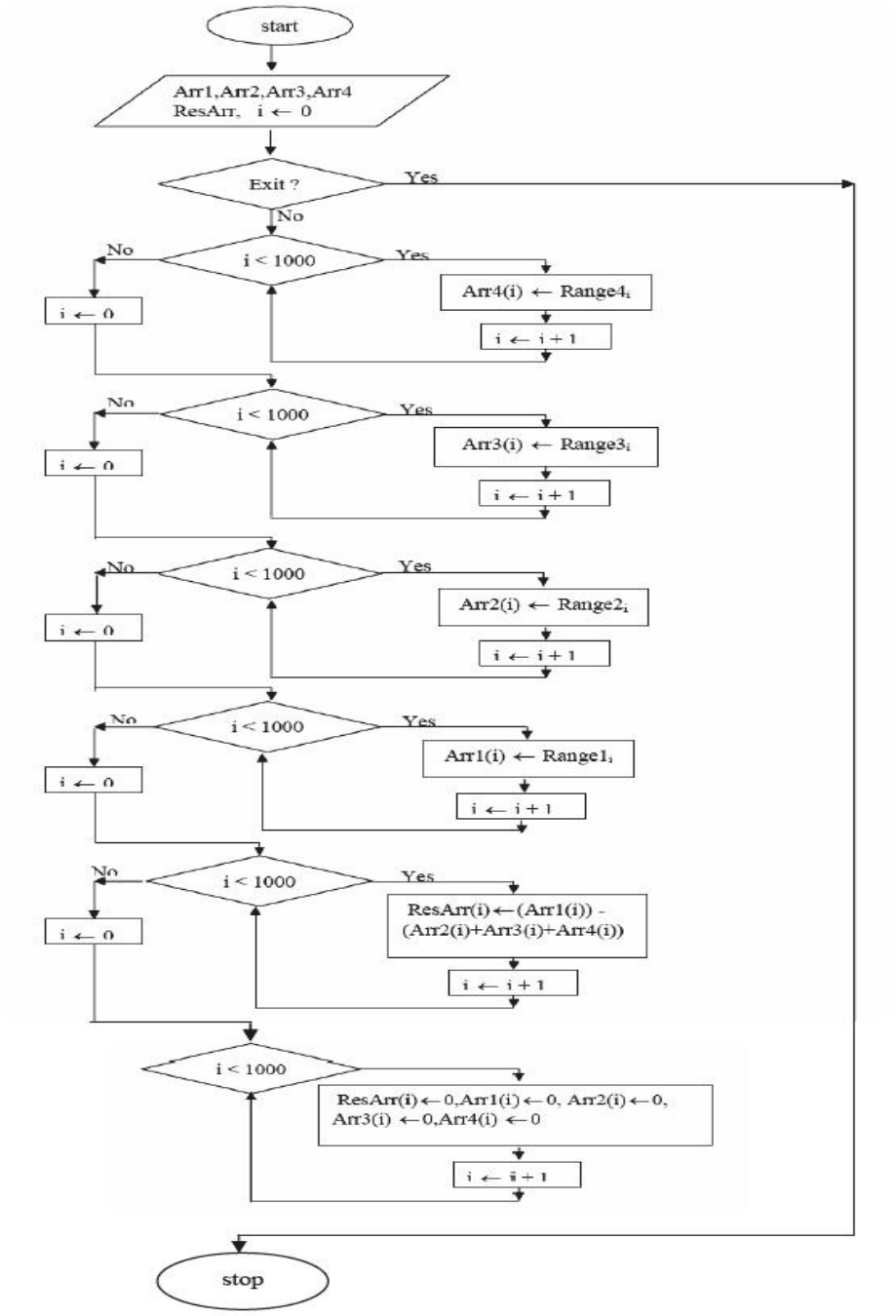


Figure 3.5 Flow chart for storing ranges.

3.4 Conclusion

In this chapter, we have shown a new technique of implementing a digital beamformer which produces exceptionally narrow footprint. The concept used here is

SUM-3×DIFFERENCE, where SUM is the signal received after reflection from moving object and DIFFERENCE is the surroundings of moving object which results in very narrow beam. Assuming that the target is approaching/receding the radar from broadside direction. The data received from each range gate is stored in a single dimensional array. The addition/subtraction is performed in real time on these stored numbers. The net result of such operation displays negative values in amplitude over a large range of elevation angle other than broadside. If negative values are discarded, we will have a very narrow visible angle along with elimination of signal received from direction other than desired angle.

CHAPTER-4

FREQUENCY ALLOCATION IN THE SOFTWARE DEFINED RADIO

4.1 Introduction

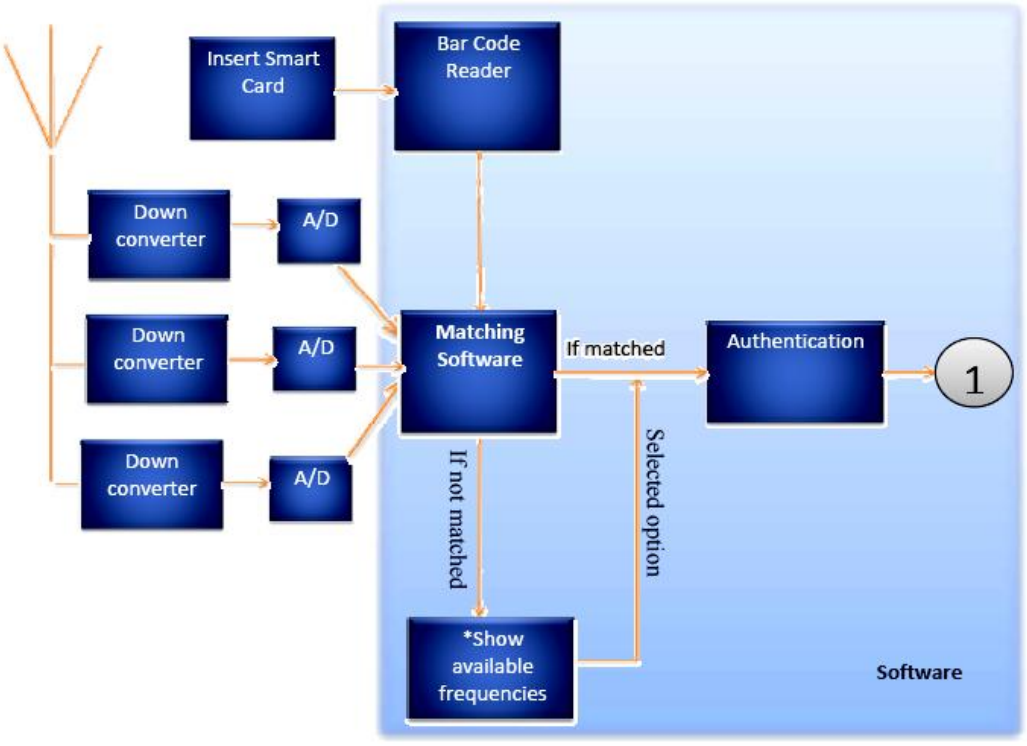
The portability of software for every frequency that has to be received using the SDR, keeping in mind the security concerns is a major issue for discussion at present. A smart card provides the portability and flexibility feature on which a transmission medium can be defined. But security still remains a concern. The need exists for a security mechanism so as to bring safe software radio transmission a reality. In this chapter we provide a mechanism to solve the problem of SDR (Efstathiou et al, 1999) transmission security and portability by implementing its software on a compact smart card using an authentication service which implements a cryptographic algorithm. Smart cards are essentially devices that allow information storage and processing. The microcontroller used in smart card applications contains a central processing unit (CPU) and blocks of memory, including RAM, ROM, and reprogrammable non-volatile memory usually electrical erasable programmable read only memory (EEPROM) or Flash-EEPROM. RAM is used to store executing programs and data temporarily, while ROM will be used to store the operating system (Won et al, 2002), fixed data, and standard routines. The re-programmable non-volatile memory is used to store information that to be retained when power is removed, but that must also be alterable to accommodate data specific to individual that has to be retained when power is removed, but that must also be alterable to accommodate data specific to individual cards or any changes possible over their lifetimes; more specifically, the smart card non volatile memory (NVM) constitutes the data storage for the database. Based on this consideration, technology issues have a significant impact on the overall system performance. Today's micro-controllers contain a CPU, memory including about of 196 KB of ROM, 8 KB of RAM and 128 KB of EEPROM. The operating system is typically stored in ROM, the CPU uses RAM as its working and most of the data is stored in EEPROM. We must also notice that the particular

features of flash memories make smart card databases differ from main memory databases, where flash memory acts as a true secondary storage with very different read/write proprieties which respect the RAM main memory, making it look more like a traditional data base management system (DBMS).

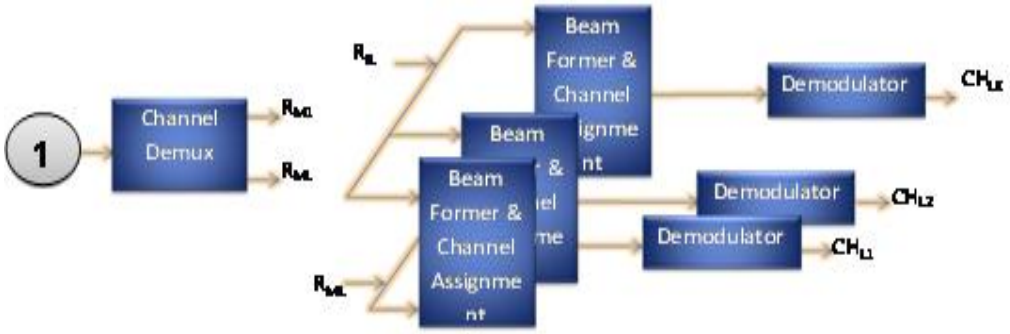
We can incorporate a flash memory inside a smart card and a number of devices like a micro SD card, which come in very compact sizes, can be actually fixed on a smart card. Inside this memory device, we can store the installation packages for different software which take care of different range of frequencies. Appropriate software will be loaded on authentication of a particular frequency to which it is tuned to. Flash memory is among the top choices for the storage media in ubiquitous computing. With a strong demand of high capacity storage devices, the usages of flash memory quickly grow beyond their original designs.

Flash memory is non volatile, shock-resistant, and power economic. With the recent technology breakthroughs in both capacity and reliability, flash-memory storage systems are much more affordable than ever. As result, flash-memory is now among the top choices for storage media in ubiquitous computing. Researchers have been investing how to utilize flash-memory technology in existing storage systems, especially when new challenges are introduced by the characteristics of flash memory. With the rapid growing of the flash memory capacity, severe challenges on the flash memory management issues might be faced, especially guarantee of security. There are two major types of flash memory: NAND flash and NOR flash. The NAND flash memory is specially designed for data storage, and the NOR flash is for EEPROM replacement. A NAND flash memory is organized in terms of blocks, where each block is of a fixed number of pages. A block is the smallest unit for erase operations, while reads and writes are processed in terms of pages. The typical block size and the page size of a NAND flash memory are 16 KB and 512KB, respectively. There is a 16-byte "spare area" appended to every page, where out-of-band data could be written to the spare areas. One of the main reasons for implementing the model using a smart card with integrated flash memory is that it makes software piracy an impossible task.

4.2 Schematic Diagram of SDR



(a)



(b)

Figure 4.1(a) Block diagram of the proposed SDR system and (b) software end for a base station.

After the antenna tuned to a radio frequency receives a frequency band (Yang Lie-Liang and Hanzo, 2002), the signals will be forwarded to ADC converters, one for each frequency block. The ADC converts the signal to a digitized form and this digital format of a signal will be the input on a PC. A smart card is available to the authorized user who inserts this card in a PC. The card will be tuned to a certain

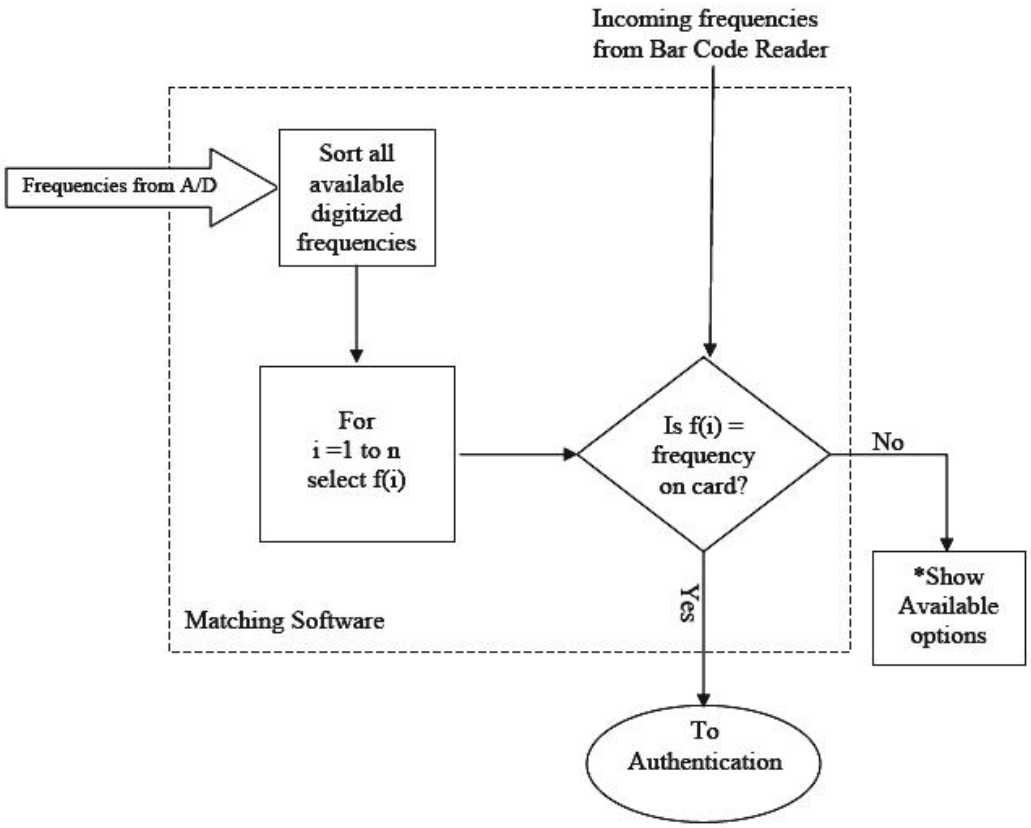
digitized code that will correspond to some particular frequency (Borio et al, 2008) that is received from the ADC converter. A Matching Software explained later in this thesis will match the received digital signal to the digitized image provided on the smart card. If match is found, an algorithm will be used to authenticate the card provided by the user. The user will be asked to input his smart card number and a secret personal identification number (PIN) which only he is provided with. If authenticated, the user will be able to process or simply retrieve the signals received for which he is a member.

If the matching software is not able to find a corresponding match for the smart card code, it will display a list of available frequency which can be tuned. If the user has a corresponding membership, he can tune his smart card to that particular frequency (Staszewski et al, 2005) and again request for the match. The next phase will be authentication and demultiplexing of the channel received for further processing in software.

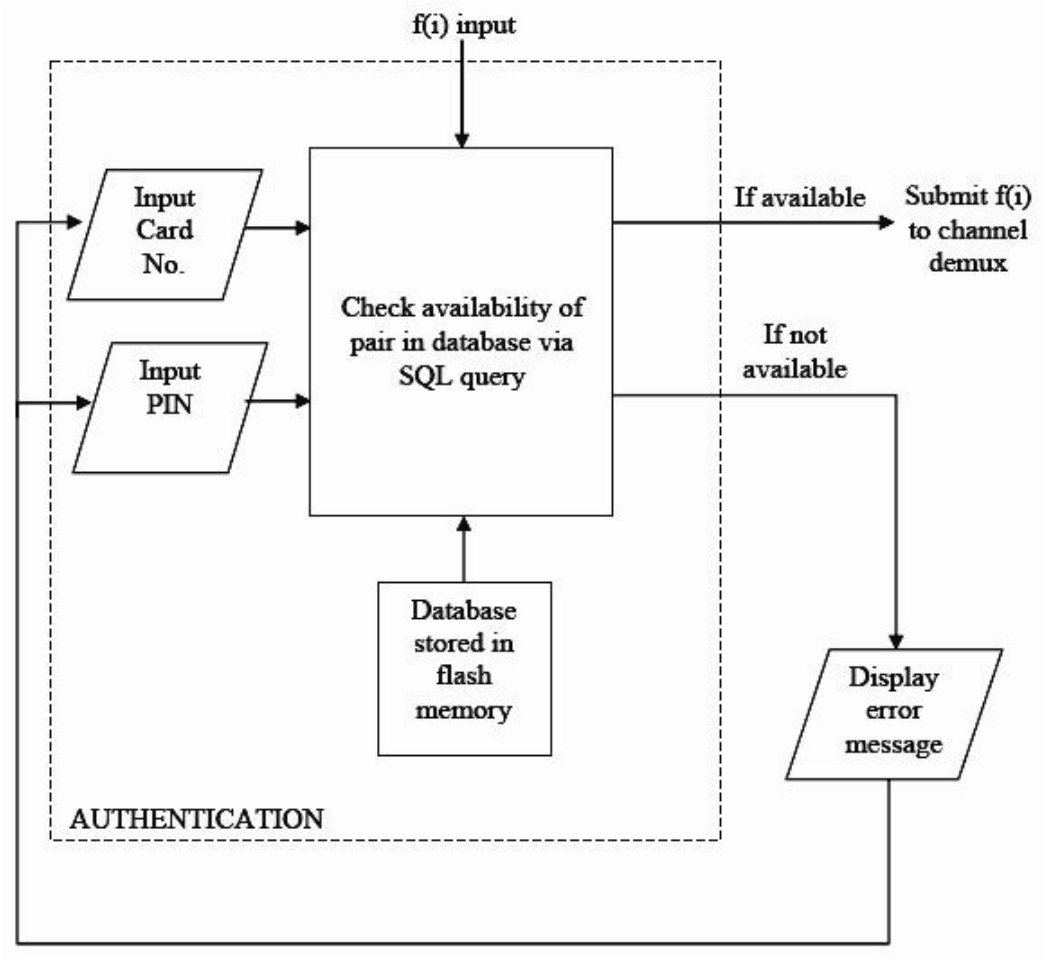
The functional block diagram of the software radio with smart antennas (Winters, 1998) is shown in above Figure 4.1(a) and Figure 4.1(a). Each antenna element has its own down-converter and ADC.

4.3 Matching Software

Figure 4.2 (a) shows a flowchart for the Matching Software proposed. The input to the software will consist of the range on frequencies received from ADC converters as well as the digitized frequencies from the bar code reader. The digitized frequencies coming from the ADC converter are first sorted. After that for each frequency, it will decide whether it is similar to the digitized frequency it is reading from the bar code reader or not. If matched, the frequency will be forwarded to the authentication software. If not, it will move to the next received frequency and match it. If no corresponding match is found, a new software module will display the list of available frequencies and the user will be asked to make a new choice and tune his smart card to any new available frequency.


Incoming frequencies
from Bar Code Reader
Frequencies from A/D
Sort all
available
digitized
frequencies
For
i =1 to n
select f(i)
Is f(i) =
frequency
on card?
No
*Show
Available
options
Yes
Matching Software
To
Authentication

(a)



(b)

Figure 4.2(a) Flow chart for the proposed matching software (b) Block diagram for the proposed authentication model.

4.4 Authentication

The block diagram in Figure 4.2(b) takes input in the form of digitized frequencies from the Matching Software. Also it prompts the user for the card number provided to the user on the smart card as well as the PIN secretly known only by the user. When the user submits the required information, an SQL query will be formed from the same to find a corresponding match pair in the database provided on the card that is integrated in flash memory. This database can be updated each time the authentication is granted and the signal are received as the authority manufacturing the product will be transmitting this in the form of radio signals at all time. After the authentication is granted, the matched digitized frequency will be forwarded to the channel demux. If

no corresponding match is found in the database for the submitted query, the software will prompt an error message to the user and show request for entering the authentication details that is card No. and secret PIN again. After some specified number of trail given to the user, the card may be blocked.

4.5 Results and Discussion

We have proposed an idea for the solution to differentiate between two close frequency transmitted by two different stations where they disturb the signal of each other. We also use adaptive beamforming with smart antennas (Banbury, 2004) at the receiver increases the carrier-to-interference ratio (CIR) in a wireless link. Due to recent advances in high-speed DSPs and ADCs, the commercial implementation of SDR (Harris and Rice, 2001) has become viable. In SDR systems, the IF signals is digitized using wide-band ADCs and all of the subsequent processing have been implemented in software. The main advantage of software radio is its great flexibility such that it can be programmed for emerging standards. It also can be dynamically updated with new software without any changes in hardware infrastructure. In wireless applications (Du, 1998) where different standards might be deployed, user's roaming can be a big issue in existing platforms. In the SDR system, user's just need to download the new air interface upon entering the new territory. The reallocation of bandwidth is a standards-setting process that takes a considerably long time. On the other hand, due to fixed finite resources, one cannot assume that more physical radio channels will be added to a spectrum allocation as shown in Figure 4.3 to reduce the probability of blocking or forced termination. The increasing popularity of wireless communication services together with the limited amount of the available radio spectrum calls for highly efficient usage of resources in the system. The interference reduction capability of antenna arrays has been considered as a means to increase the capacity of wireless systems (Vitturi et al, 2007). Specifically, using beam forming techniques at the receiver, two or more transmitters can share the same traffic channel to communicate with the base station at the same time. An adaptive antenna (Widrow and Stearns 1985, Swales et al, 1990), array is used at the base station to form several antenna beams simultaneously. Each beam captures one transmitter by automatically pointing its pattern toward that transmitter while nulling other co-channel transmitters

and multipath signals. In this way, the Co-channel interference (CCI) is minimized, and therefore the CIR for the signal of interest is maximized. In urban wireless environments, the signal transmitted by each user is reflected by surrounding buildings and the terrain. Therefore, several copies of the transmitted signal are received at the base station with different delays and different attenuation. This effect is called multipath fading. In space-only diversity, given a cell with channels, an - element antenna array that forms distinct array nulls at the receiver. It allows a maximum of users to be served in a cell. Multipath factor representing the number of distinct strong path components received from each mobile station is fed at the beam forming array. In space–time diversity, spatial nulls reject the CCI, ISI is eliminated by time diversity. Sectorization is an alternative to smart antennas (Kennedy and Sullivan, 1995). Sectorized cell sites employ hardware beam forming array antennas in which each beam is assigned a distinct RF channel set. The direction and gain of sectorized antennas are fixed in the hardware. They cannot place nulls on interference like the smart antenna (Seungheon et al, 2008). The cost of a sectorized cell site is an increase in the analog hardware complexity of the cell site, but there is virtually no impact on the single-channel cell site software. When the capacity of a sectorized site is exceeded, one may then overlay a smart antenna, with its dedicated DSP capacity and unique software architecture which accommodates the vastly increased computational demand of the beamforming network.

But the subsequent beamforming and demodulation (Rashid-Farrokhi et al, 1996, Javad et al, 1999) are implemented in software and are shared among all of the elements. The smart antenna's beams are not fixed, but are dynamic per user, and will place nulls that cancel interference. Another advantage of the smart antenna system is the reduced rate of handoffs because of tracking the user. The term "cell" means either a conventional cell or one sector of a sectorized cell (Swales et al, 1990). Two potential applications show the advantages of a system with a smart antenna. First, a wireless network with beamforming capabilities at the receiver allows two or more transmitters to share the same channel to communicate with the base station. Each cell is modeled by a multi-user multi server service facility. Each server is for beamforming and channel forming used in the base station of the cell. For a set of co channel transmitters, the probability of successful capture by a separate antenna beam

is computed. The success probabilities are taken into account in the queuing model of the system. From this generalized model, the closed-form blocking probabilities of the calls and total carried traffic in the system under different traffic policies are derived. The second application shows how to implement a robust power control algorithm when using a smart antenna at the base station. In CDMA networks (Everitt, 1994), power control is an important issue because of the near–far effect. Therefore, the effective power control algorithm results in a "capacity increase" in the system. There is a problem if frequencies of two channels are very close to each other. If there frequencies are very-very close then there may be some disturbance in receiving their signals at the receiver end.

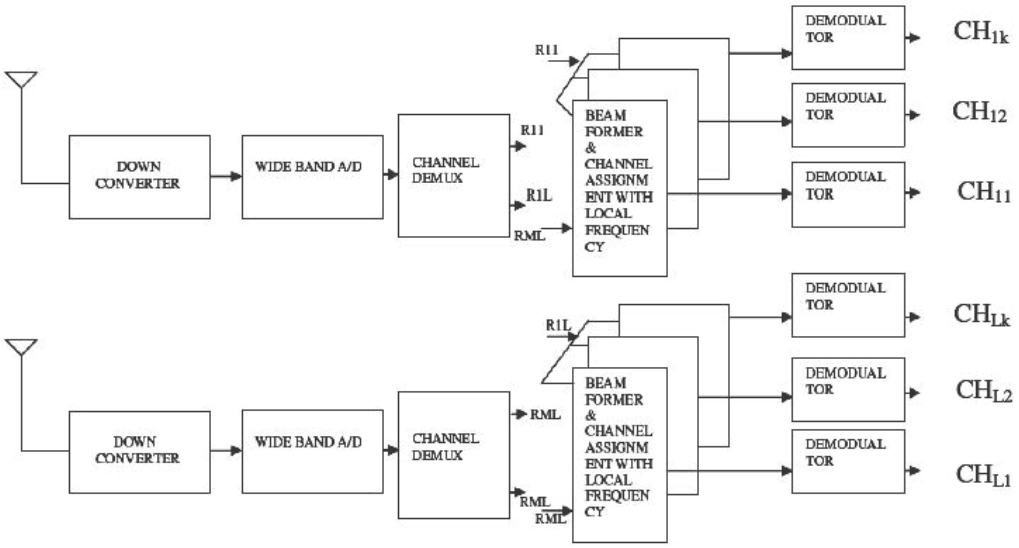
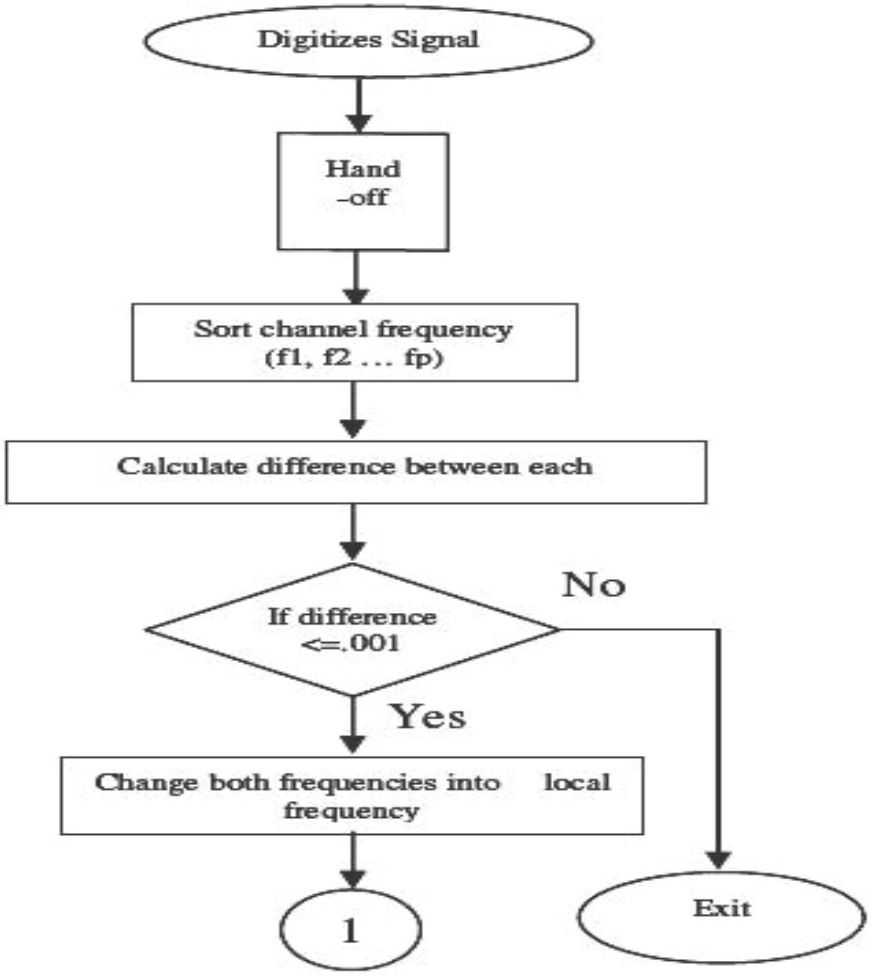


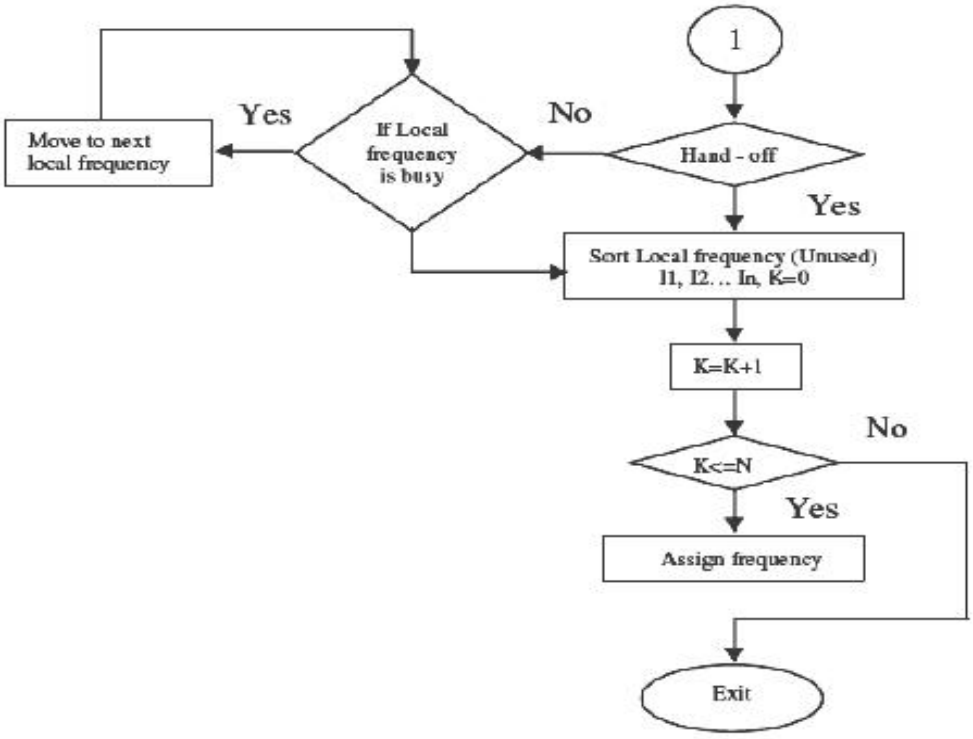
Figure 4.3 Functional block diagram of software radio for a base station with smart antenna.

A wide-band front-end (Wikborg et al, 1999) down converters the received signal to the IF where it is sampled and digitized by a high-speed ADC. The rest of the processing is implemented in software. Such a radio may be dynamically updated with new software without changes in hardware and infrastructure. One may achieve better performance by introducing coding on the bit stream using coding gain to improve the bit-error rate (BER). In the case of the omni-directional antenna, the software of the cell site may either have an IF software radio architecture (Alsolaim et al, 2000) in which the waveforms are synthesized and received in software, or they

may have a base band DSP radio architecture, in which the software is limited to bit stream signal processing.



(a)



(b)

Figure 4.4(a) Flow chart for checking the channels that whether they are assigning into a local frequencies or not (b) Flow chart for changing incoming frequencies into the local frequencies.

From Figure 4.2(a) and Figure 4.2(b), we can assign any two frequencies into unused local frequencies. We are checking for the frequencies which are closer to each other and due to this closeness they are disturbing their signals which are transmitted by their respective transmitter. Here we firstly sort all the channel frequencies and sort it into increasing order, and then we are checking the difference between every frequency. Here we assume that if difference between any two frequencies is less than 0.001 then they will disturb each other. After checking these differences, if any difference is less than 0.001 then we change those frequencies into local frequencies which are defined in Figure 4.4 (a). In Figure 4.4 (b) we check whether local frequencies have already in use or not that is. hand off condition. If it is used and local frequencies have already assigned to any other frequency, then it will move to next frequency and it will check till it does not found any free local

frequency. If there is handoff condition then it will detect all the available local frequencies and assign these local frequencies to the incoming frequencies.

4.6 Conclusion

In this chapter, we have proposed the design of SDR that implements its frequency allocation by using smart cards. Smart cards are essential device that allows information storage and processing. This approach concern with security and trashes all aspect of potential privacy in software distribution. The technology of the SDR is still picking up but promises a great revolution in digital communication. In future, not only the hardware will be replaced with software but antenna array will be capable of receiving and transmitting different air interface by auto-reconfigure elements. Thus an antenna integrated with open-source software will make it possible to create an ideal and complete SDR.

CHAPTER-5

REAL-TIME IMPLEMENTATION OF PROGRAM BY USING TMS320C6713 DSK PROCESSOR

5.1 Introduction

Digital signal processors such as the TMS320C6x (C6x) family of processors are like fast special-purpose microprocessors with a specialized type of architecture and an instruction set appropriate for signal processing. Digital signal processors are used for a wide range of applications, from communications and controls to speech and image processing (Chassaing, 2005). The general-purpose digital signal processor is dominated by applications in cellular communications. Applications embedded digital signal processors are dominated by consumer products. These processors have become the products of choice for a number of consumer applications, since they have become very cost-effective. They can handle different tasks, since they can be reprogrammed readily for a different application. DSP techniques have been very successful because of the development of low-cost software and hardware support. For example, modems (Yang and Lin, 2006) and speech recognition can be less expensive using DSP techniques. DSP processors are concerned primarily with real-time signal processing. Real time (Murotake et al, 2000) processing requires the processing to keep pace with some external event, whereas non-real-time processing has no such timing constraint. The external event to keep pace with is usually the analog input. Whereas analog-based systems with discrete electronic components such as resistors can be more sensitive to temperature changes, DSP-based systems are less affected by environmental conditions.

DSP processors enjoy the advantages of microprocessors. They are easy to use, flexible, and economical. The basic system consists of an ADC (Salkintzis et al, 1999) to capture an input signal. The resulting digital representation of the captured signal is then processed by a digital signal processor such as the C6x and then output through a digital-to-analog converter (DAC). Also included within the basic system are a special

input filter for anti-aliasing to eliminate erroneous signals and an output filter to smooth or reconstruct the processed output signal.

The TMS320C6713 (C6713) is based on the very long instruction word (VLIW) architecture, which is very well suited for numerically intensive algorithms. The internal program memory is structured so that a total of eight instructions can be fetched every cycle. For example, with a clock rate of 225MHz, the C6713 is capable of fetching eight 32-bit instructions every 1/(225 MHz) or 4.44 ns.

Interoperability concerns and high-cost, associated with existing communication systems, are driving the integration or SDR (Rauwerda et al, 2008) technology into commercial and military wireless systems. In the original context, the form SDR refers to a reconfigurable radio based solely on software and having the ADC (Araujo and Dinis, 2007, Gulati and Lee, 2001) occurring directly at antenna (Zhang et al, 2008), while practical limitation in the current performance of ADC (Walden, 1999, Wepman, 1995) prevent sampling wideband waveforms directly at antenna, the development of a radio system that can change the operating frequency, modulation, operating bandwidth and network protocol (Yang and Qi, 2006) without the need to change the system hardware is highly desirable.

The SDR (Mitola, 1995) is a flexible architecture allowing multiple waveforms to be rapidly ported. It is a communications device whose functionality is defined in software. Defining the radio behaviour in software removes the need for hardware alterations during a technology upgrade (Mitola and Zvonar, 2001, Bagheri et. al., 2006). In order to maintain interoperability, the radio systems must be built upon a well-defined, standardized, open architecture. Defining the architecture also enhances scalability and provides plug-and-play behaviour for the components of a radio. SDR (Kenington, 1999) converts analog signals into digital data to be processed by the various computing resources within the radio platform software controls.

- Transmit and receive frequencies.
- Selects the desired bandwidth.

Performs the transmit gain control (TGC) and automatic gain control (AGC) functions.

- Sets and monitors the output power level.
- Provides system fault handling.

- Provides the man-machine interface (Yang and Wang, 2006).

The encryption software process configures and monitors security with a recent trend toward performing the entire encryption process in software. Networking aspects (Dorai and Yeung, 2002) of the data traffic are either completely or partially implemented in software. Finally, the man-machine interface (Ju and Xiaoguang, 2000) is completely defined within a software process allowing adaptability to new capabilities with an emphasis on simplifying radio to user interaction

Thus in SDR cent percent of the modulation and demodulation is defined in software instead of being hardwired into the electronics (Bose et. al., 1999). This means that the frequency band, performance, and functionality can be upgraded with a simple software download (Cummings and Heath, 1999) and update. In essence, an SDR is a radio that is substantially defined in software, with a physical layer (Akan and Akyildiz, June 2004, Markwalter and Fitzpatrick, 1989) behaviour that can be significantly altered through changes to its software. SDR provides an efficient and comparatively inexpensive solution to the problem of building multimode, multiband, multifunctional wireless devices. An SDR (Valls et al, 2006) is capable of being reconfigured to operate with different waveforms and protocols through dynamic loading of new waveforms and protocols (Mitola et. al., 1999, Coy et al., 1992).

5.2 Talk-Through Application

Our goal is to pass the signal entering the ADC (Luschas et. al., 2004) directly to the DAC, without actual processing being performed. This process is called Talk-Through. Ideally, the reconstructed analog signal coming out of the DAC should be identical to the analog input signal that went to the ADC. For this purpose we used TMS320C6713DSK kit for digital signal processing (Marhaban, 2006).

5.2.1 Output

If an audio source is connected to the digital signal processing kit (DSK) audio input and a pair of speakers connected to the audio output, whatever music is given as input shall be heard as output. In case the output signal sounds fuzzy, distorted, or clipped the ADC might be overdriven. For example the pulse coded modulation (PCM) 3006 has a maximum input voltage of about ± 1. If the input signal exceeds this range, the

signal will sound fuzzy, distorted or clipped. The application permits three basic effects:

a) Quantization

The effect of different bit length conversions can be shown by the variable truncation of the audio data, reducing the effective resolution of the codec converters to minimum of one bit.

b) Spectral inversion

By selecting the invert spectrum checkbox, the sign bit of every other sample is changed. This is equivalent to modulating the input signal with a frequency of one half of the sample frequency (Luse, 1988). The effect is that the frequency spectrum is flipped around a frequency equal to the sample frequency divided by four, effectively "scrambling" the signal as it would be heard by the listener. If the resulting signal is then passed through a second DSK performing the same operation, the original signal will be recovered.

c) Aliasing

The effective sampling rate can be varied by using a variable decimation factor and a single input sample is repeatedly transmitted for an integral number of output samples, which reduces the effective sample rate of the converter by that integral number. In this way aliasing can be easily demonstrated even when using a sigma-delta converter.

5.2.2 AIC23 codec

The DSK uses a Texas Instruments AIC23 (part #TLV320AIC23) stereo codec for input and output of audio signals. The codec samples analog signals on the microphone or line inputs and converts them into digital data so it can be processed by the DSP. When the DSP is finished with the data it uses the codec to convert the samples back into analog signals on the line and headphone outputs so the user can hear the output. The codec communicates using two serial channels (Di-Stefano,

1987), one to control the codec's internal configuration registers and one to send and receive digital audio samples.

The McBSP in the digital signal processors (DSPs) of the TMS320C6000 DSP family. Association of all the chip of DSK is shown in Figure 5.1(a) (Spectrum Digital, 2003). How the different values are set of Figure 5.2 is shown in the programming part.

The McBSP provides these functions:

1. Full-duplex communication.

2. Double-buffered data registers, which allow a continuous data stream.

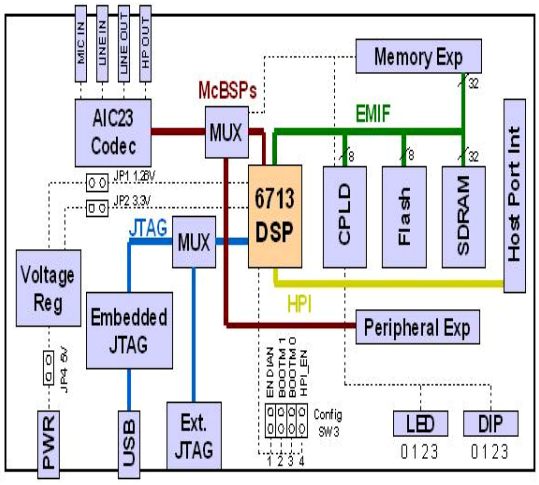
3. Independent framing and clocking for receive and transmit.

4. Direct interface to industry-standard codec, analog interface chips (AICs), and other serially connected ADC and DAC devices.

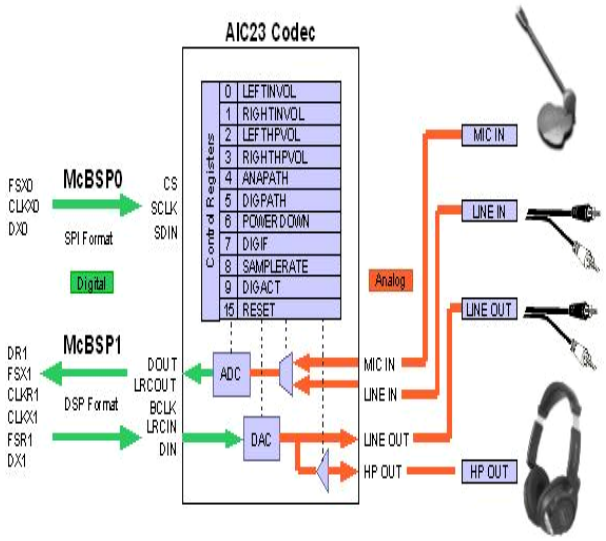
5. External shift clock or an internal, programmable frequency shift clock for data transfer.

It has two ports, namely McBSP0 and McBSP1 (Asif et. al., 2005). McBSP0 is used as the unidirectional control channel. The control channel is only used when configuring the codec, it is generally idle when audio data is being transmitted, McBSP1 is used as the bi-directional data channel. All audio data flows through the data channel.

1. Configuring The AIC23 Codec



(a)



(b)

Figure 5.1(a) Different chips in main DSK Kit (b) Interfaces with CODEC.

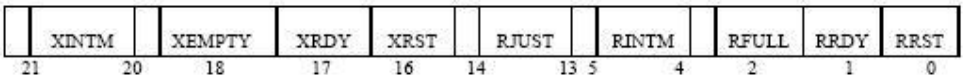


Figure 5.2 Serial Port Control Register (018C0004h)

First phase:

The codec samples analog signals on the microphone or line inputs and converts them into digital data so it can be processed by the DSP, when the DSP is finished with the data it uses the codec to convert the samples back into analog signals on the line and headphone outputs so the user can hear the output.

Second phase:

Implemented certain real time programs, in which we receive real-time frequency modulated signals onto the TMSC6713DSK processor (Ozbay and Kavsaoglu, 2010) and process the incoming signals and reflect the output desired. FM receiver (Zumbul et al, 2008) was constructed and then the signal received from the receiver was forwarded to the DSK processor and proposed a method for authentication and transmission security for over-the-air (OTA) software download sequence (Gallery, 2003).

The following code demonstrates the configuration of the AIC23 CODEC.

```
#include "C:\CCStudio_v3.1\C6000\dsk6713\include\dsk6713.h"
#include "C:\CCStudio_v3.1\C6000\dsk6713\include\dsk6713_aic23.h"
DSK6713_AIC23_Config config = DSK6713_AIC23_DEFAULTCONFIG;
DSK6713_AIC23_CodecHandle AIC23_handle;
/* Configuring the Codec AIC23 */
void DSK6713_AIC23_conf()
{
/* reset and Configure the rest of the AIC23 registers */
AIC23_handle = DSK6713_AIC23_openCodec(0, &config);
DSK6713_AIC23_setFreq(AIC23_handle, 48000); //set sample rate
}
```

DSK6713_AIC23_openCodec().

This function configures serial port McBSP0 to act as a unidirectional control channel in the serial peripheral interface (SPI) mode transmitting 16-bit words. Then configures the AIC23 stereo codec to operate in the DSP mode with 16-bit data words with a sampling rate of 48 kHz then McBSP1 is configured to send data samples to the codec or receive data samples from the codec in the DSP format using 32-bit words. The first word transmitted by the AIC23 is the left channel sample. The right channel sample is transmitted immediately after the left sample. The AIC23 generates single frame sync at the beginning of the left channel sample. Therefore, a 32-bit word received by McBSP1 contains the left sample in the upper 16 bits and the right sample in the lower 16 bits. The 16-bit samples are in 2's complement format. Words transmitted from McBSP1 to AIC23 must have the same format. The codec and McBSP1 are configured so that the codec generates the frame synchronization and shift clocks as shown in Figure 5.1(b) (Spectrum Digital, 2003).

2. AIC23 sampling rates

The C6713 DSK (Egami, 2006) supplies a 12 MHz clock to the AIC23 codec which is divided down internally in the AIC23 to give the sampling rates shown in the table below. The codec can be set to these sampling rates by using the function DSK6713_AIC23_setFreq(handle, freq ID).

3. AIC23 Analog Interface Properties

- Line Inputs
  - ADC full-scale range of 1.0 V RMS
- Microphone Input
  - MICIN is a high-impedance, low-capacitance input compatible with a wide range of microphones.
- Line Outputs
  - DAC full-scale output voltage is 1.0 V RMS.
- Headphone Output
  - Stereo headphone outputs designed to drive 16 or 32- ohm headphones.
- Analog Bypass Mode
  - The analog line inputs can be directly connected to the analog line outputs.
- Sidetone Interface
  - The AIC23 has a sidetone insertion mode where the microphone input is routed to the line and headphone outputs.

5.2.3 Configure the McBSP

```
#include "mcbspcfg.h"
/* function decleration */
void DSK6713_AIC23_conf();
void main()
{
int input, i;   /* Local variable */
/* Configure AIC23 CODEC */
DSK6713_AIC23_conf();
/* Clear any garbage from the codec data port */
if (MCBSP_rrdy(hmcbsp1))
MCBSP_read(hmcbsp1);
/* Start McBSP1 as the codec data channel */
```

```
MCBSP_start(hmcbsp1,                                    MCBSP_XMIT_START|
MCBSP_RCV_START|MCBSP_SRGR_START|
MCBSP_SRGR_FRAMESYNC, 220);
while(1)     /* Endless loop IO audio codec */
{
/* Read 32 bits of codec data, loop to retry if data port is busy */
while(!MCBSP_rrdy(hmcbsp1)); /* Polling for RBR Full */
input = MCBSP_read(hmcbsp1); /* Read input data */
/* Write 32 bits to the codec, loop to retry if data port is busy */
while(!MCBSP_xrdy(hmcbsp1)); /* Polling for XBR Full */
MCBSP_write(hmcbsp1,input); /* Write output data */
}
```

5.2.4 Sending samples to the codec

Left and right sample pairs are sent to the codec as 32-bit words with the left channel sample in the upper 16 bits and the right channel sample in the lower 16 bits. Each sample is in 16-bit two's complement format. These 32-bit words are sent to the codec by the BSL function:-

DSK6713_AIC23_write().

This function Polls the McBSP1 XRDY flag and returns immediately without sending the sample and also returns the value 0 if it is FALSE. It sends the sample word by writing it to the data terminal ready (DTR) of McBSP1 and returns the value 1 if XRDY is 1(TRUE).

5.2.5 Receiving samples from the codec

Words are read from the codec by using the function

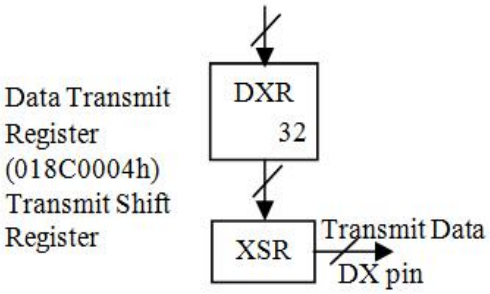
DSK6713_AIC23_read().

This function: polls the RRDY flag of McBSP1 and returns immediately if it is FALSE without reading a word and also returns the value FALSE. If RRDY is TRUE it reads a word from the Data Receive Register (DRR) of McBSP1 and returns the value TRUE.

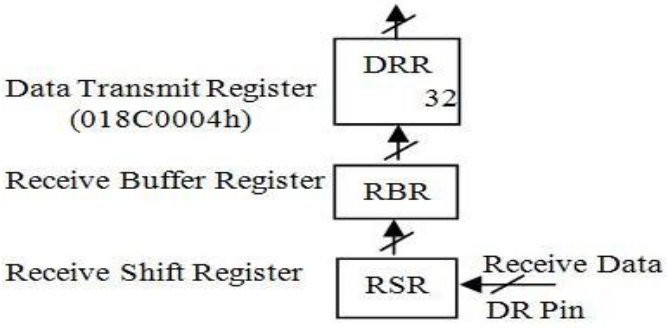
5.2.6 Multichannel buffered serial port (McBSP) properties

- Can generate shift clocks and frame sync signals internally, or externally. The DSK uses external ones.
- Can transmit or receive 8, 12, 16, 20, 24, or 32-bit words.
- Double-buffered data registers, which allow a continuous data stream.
- Can generate receive and transmit interrupts to the CPU or events to the enhanced direct memory access (EDMA) (Jian and Xing, 2008).
- Law and A-law hardware companding options.

Multichannel selection of up to 32 elements from a 128 element time division multiple access (TDMA) (Santivanez and Stavrakakis, 1999) frame which is direct interface to industry-standard codec.



(a)



(b)

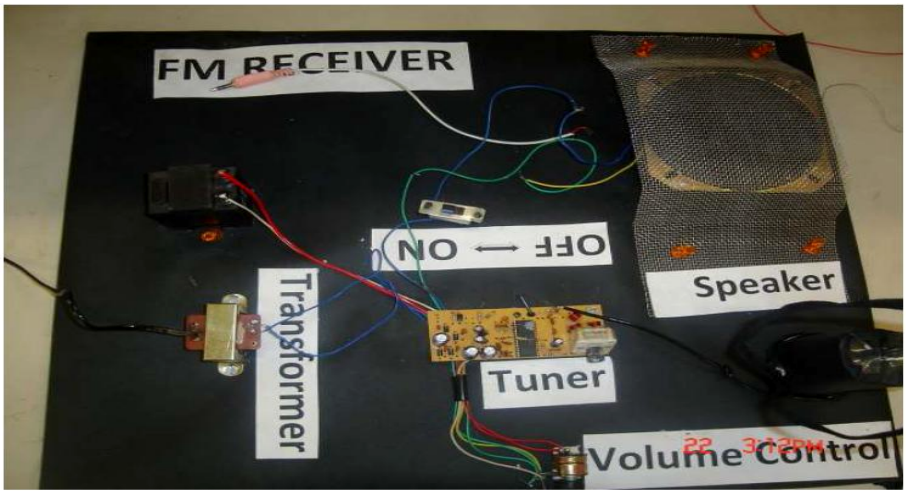
Figure 5.3 McBSP block diagram of the (a) transmitter and (b) receiver

5.2.7 Operation of serial port transmitter

- The serial port transmitter sends an interrupt request (XINT) to the CPU when the XRDY flag makes a transition from 0 to 1 then XINTM = 00b in the SPCR. It also sends a Transmit Event Notice (XEVT) to the EDMA. The CPU or EDMA writes a word into the data transmit register (DXR). The XRDY flag is cleared whenever data is written to the DXR.
- After a word (32 bits in our case) is shifted out of Transmit Shift Register (XSR), a parallel transfer of the DXR into the XSR is performed. The XRDY flag is set when the transfer occurs as shown in Figure 5.3 (a).

5.2.8 Operation of serial port receiver

- When a full element is received, the 32-bit RSR is transferred in parallel to the Receive Buffer Register (RBR) if it is empty.
- The RBR is copied to the Data Receive Register (DRR) if it is empty.
- The RRDY bit in SPCR is set to 1 when RSR is moved to DRR, and it is cleared when DRR is read.
- When RRDY transitions from 0 to 1, the McBSP generates a CPU interrupt request (RINT) if RINTM = 00b in the SPCR. A receive event (REVT) is also sent to the EDMA controller.
- RX bits shift serially into the Receive Shift Register (RSR) all the above points are figured out in Figure 5.3(b).



(a)

(b)

Figure 5.4 Hardware for interfacing (a) with DSP Kit and (b) CPU with DSP Kit.

5.3 FFT Analyzer

The SR760 FFT Spectrum Analyzer (Liguori et. al., 2004) takes a time varying input signal, like it would be seen on an oscilloscope trace, and computes its frequency spectrum. Fourier's basic theorem states that any waveform in the time domain can be represented by the weighted sum of pure sine waves of all frequencies. For some measurements which are difficult in the time domain are very easy in the frequency domain and take harmonic distortion. It is hard to quantify the distortion by looking at a good sine wave output from a function generator on an oscilloscope. When the same signal is displayed on a spectrum analyzer, the harmonic frequencies and amplitudes are displayed with amazing clarity. Another example is noise (Amer et al, Feb. 2007) analysis, looking at an amplifier's output noise on an oscilloscope basically measures just the total noise amplitude. On a spectrum analyzer, the noise as a function of frequency is displayed. It may be that the amplifier has a problem only over certain frequency ranges. Many of time domain measurements used to be done using analog spectrum analyzers. In simple terms, an analog filter was used to isolate frequencies of interest. The remaining signal power was measured to determine the signal strength in certain frequency bands. By tuning the filters and repeating the measurements, a reasonable spectrum could be obtained. An Fast Fourier Transform (FFT) spectrum analyzer works in an entirely different way. The input signal is digitized at a high sampling rate, similar to a digitizing oscilloscope. Nyquist theorem (Singh et al, 2010)

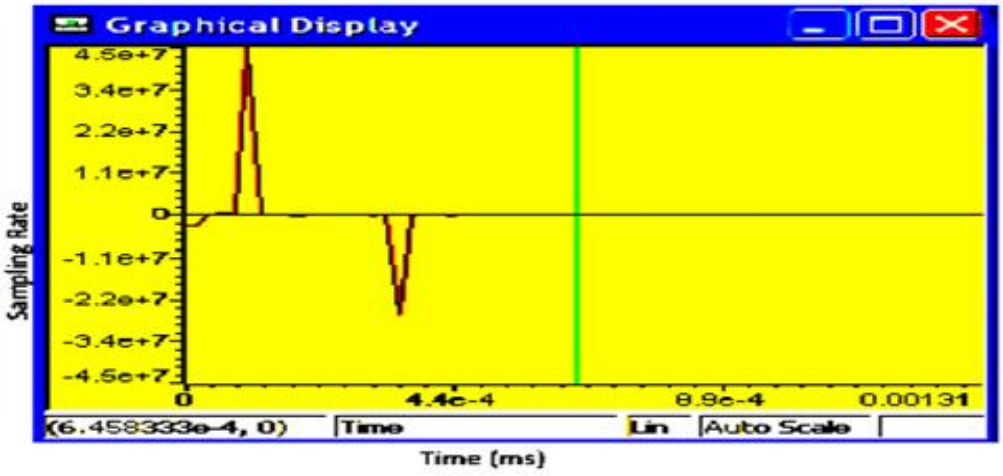
says that as long as the sampling rate is greater than twice the highest frequency component of the signal, then the sampled data will accurately represent the input signal. In the SR760, sampling occurs at 256 kHz. To make sure that Nyquist's theorem (Luse, 1988) is satisfied, the input signal passes through an analog filter which attenuates all frequency components above128 kHz by 90 dB. The resulting digital time record is then mathematically transformed into a frequency spectrum using an algorithm known as the FFT. The resulting spectrum shows the frequency components of the input signal. Now, interesting part here is the original digital time record comes from discrete samples taken at the sampling rate. The corresponding FFT yields a spectrum with discrete frequency samples. In fact, the spectrum has half as many frequencies points as there are time point points. Suppose that y 1024 samples are taken at 256 kHz. It takes 4 ms to take this time record. The highest frequency will be determined by the period of 2 time samples or 128 kHz. Hardware association with our own hardware and kit with CPU respectively are shown in Figure 5.4(a) and (b) for which we have analysed the result.

The lowest frequency is just the period of the entire record or 1/ (4 ms) or 250 Hz. The output spectrum thus represents the frequency range from DC to 128 kHz with points every 250 Hz. Figure 5.5(a) is the time domain graph, a graphical representation of the signal, with acquisition buffer size 64 and the display data size as the same. The sampling rate is set to 48000. The problem faced in the time domain graph is that some measurements are very difficult which are comparatively easy in the frequency domain. As an example, take the case of noise analysis, on the spectrum analyzer, the noise as a function of frequency is displayed.

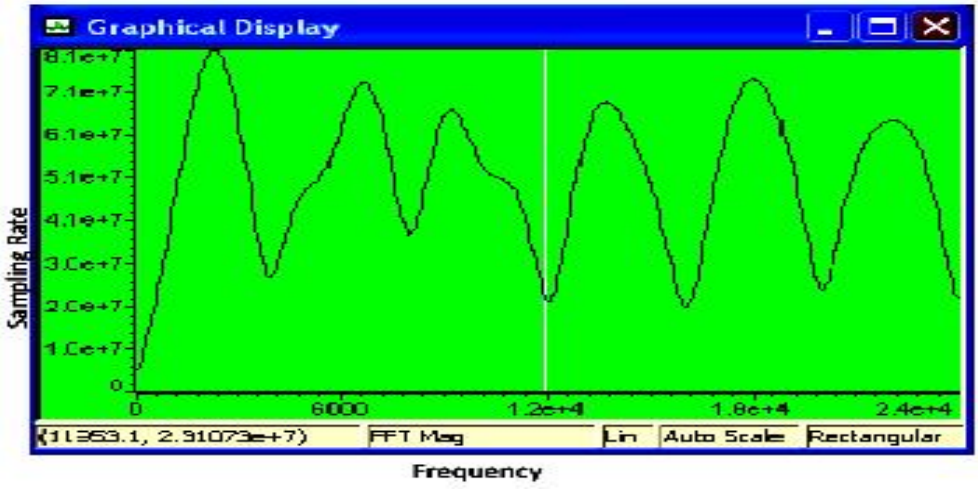
5.4 Results and Discussion

In the present real time program measurement, the entire spectrum takes only 4 ms to measure. The limitation of this measurement is its resolution, because the time record is only 4 ms long, the frequency resolution is only 250 Hz. Suppose the signal has a frequency component at 260 Hz. The FFT spectrum will detect this signal but place part of it in the 250 Hz point and part in the 500 Hz point. One way to measure this signal accurately is to take a time record that is 1/260 or 3.846 ms long with 1024 evenly spaced samples. Then the signal would land all in one frequency bin but this

would require changing the sampling rate based upon the signal which is not measured yet, which is not a good solution. In fact, the way to measure the signal accurately is to lengthen the time record and change the span of the spectrum.



(a)



(b)

Figure 5.5 Graph display of signal received in (a) the time domain and (b) frequency domain after FFT.

Figure 5.5(b) is the FFT magnitude graph, and works in an entirely different way. The input signal is digitized at a high sampling rate, similar to digitizing an oscilloscope. In the SR760, sampling occurs at 256 kHz. To make sure that Nyquist

theorem is satisfied, the input signal passes through an analog filter which attenuates all frequency components above128 kHz by 90 dB.

Figure 5.6 clearly depicts the operation of registers and its values and Figure 5.7 shows the circuit diagram of the receiver used in real time signals. This circuit receives the real-time signals and forwards them through a jack to the line in port of the DSK6713. The corresponding FFT yields a spectrum with discrete frequency samples. In fact, the spectrum has half as many frequency points as there are time points. In future many functions such as down-conversion, demodulation, security measure, spectrum analysis etc. (Singh et al, 2008) will be done by SDR (Taneja et al, 2008, Singh et al, 2008).

The advantage of this technique is its speed. The entire spectrum takes only 4 ms to measure. The limitation of this measurement is its resolution. Because the time record is only 4 ms long, the frequency resolution is only 250 Hz. The SR760 FFT Spectrum Analyzer takes a time varying input signal, which is seen on an oscilloscope trace and computes its frequency spectrum. Fourier's basic theorem states that any ate waveform in the time domain can be represented by the weighted sum of pure sine waves of all frequencies. If the signal in the time domain as seen on an oscilloscope is periodic, then its spectrum is probably dominated by a single frequency component and the spectrum analyzer represents the time domain signal by its component frequencies.

DSK6713_AIC23_write():

Left and right sample pairs are sent to the codec as 32-bit words with the left channel sample in the upper 16 bits and the right channel sample in the lower 16 bits polls the McBSP1 XRDY flag and returns immediately without sending the sample if it is false and also returns the value 0. It sends the sample word by writing it to the DXR of McBSP1 if XRDY is 1 (TRUE) and returns the value 1.

DSK6713_AIC23_read():

Polls the RRDY flag of McBSP1 and returns immediately if it is FALSE without reading a word and also returns the value FALSE. If RRDY is TRUE it reads a word from the Data Receive Register (DRR) of McBSP1 and returns the value TRUE.

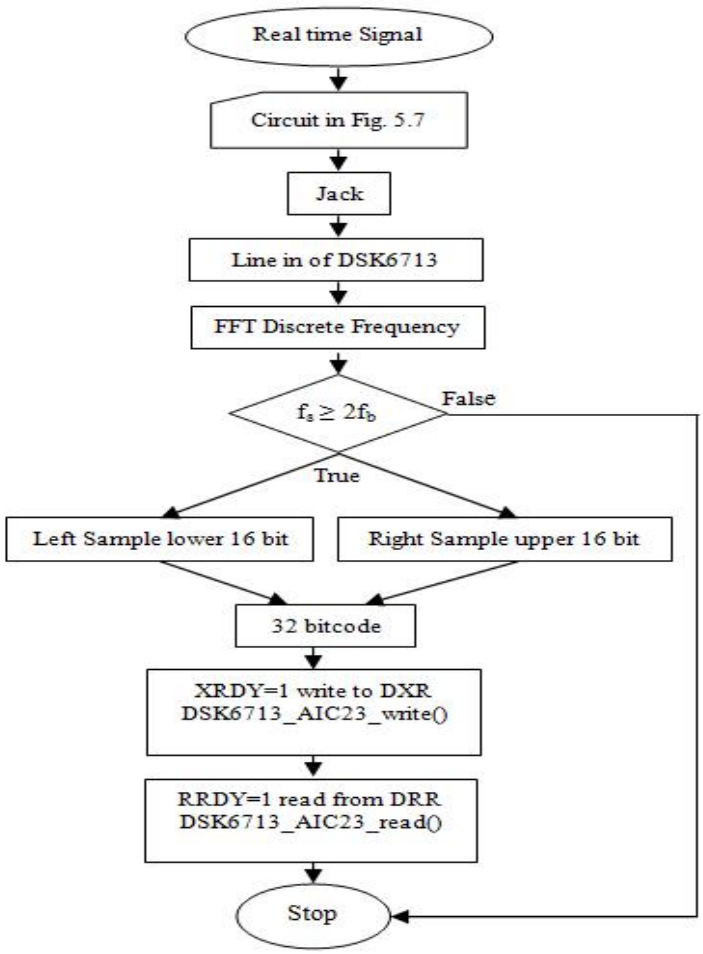


Figure 5.6 Flow chart of the read and write operation.

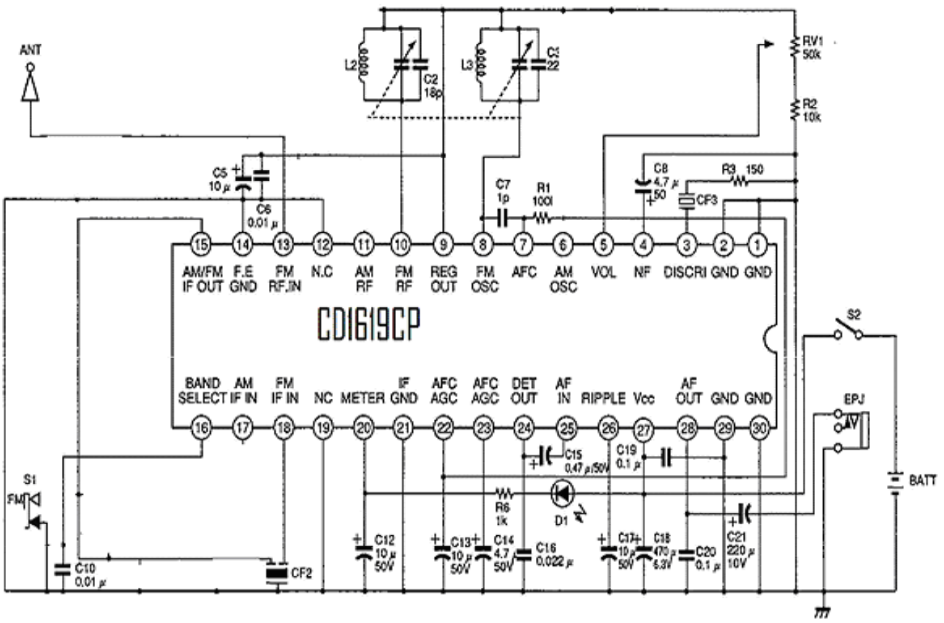


Figure 5.7 Circuit diagram of the real-time signal receiver.

5.5 Conclusion

Our hardware is accepting the radio signal by omni-antenna and then it is transferred to DSP Kit. We processed the signal by software called code-composer and did up to four time overlapping for security purpose and got the original signal back again by reversing the process.

The entire spectrum takes only 4 ms to measure. The limitation of this measurement is its resolution. Because the time record is only 4 ms long, the frequency resolution is only 250 Hz. Suppose the signal has a frequency component at 260 Hz. The FFT spectrum will detect this signal but place part of it in the 250 Hz point and part in the 500 Hz point. One way to measure the signal accurately is to lengthen the time record and change the span of the spectrum.

CHAPTER-6

WIRELESS AD-HOC NETWORK IN SOFTWARE DEFINED RADIO

6.1 Introduction

In this chapter, a novel approach is used in context with Ad –Hoc network. The parameters of communication in the ad-hoc networks changes such as the distance between nodes channel characteristics, and person who is using it changes location frequently. The Ad-Hoc network now a day is very useful. Use of radio signal makes this network more reliable and flexible because of its property. So it can be used for military purpose also. We can change software specification rather than changing any hardware such as chip every time. The change of hardware is costly and time consuming. With this reference, the SDR is economically beneficial to us. Here, we are using concept of M-ary phase shift keying (MPSK) technique for an adaptive detection. By using MPSK (Chennakeshu and Anderson, 1995), we find that MPSK signal can use two carrier signals that are perpendicular to each other for coherent detection. Implementation of MPSK adaptive detection can be done by using software programming of MPSK modulation, as it can be reprogrammed according to the requirement. SDR reduces the burden of changing the hardware so frequently, for example if an organization uses 2Mbps speed of lines and now organization need to change it to 4Mbps speed or more then all the hardware has to be changed. The same can be done using the SDR. Further, we need to change the software rather than replacing the hardware.

Software radio also provides the flexibility to adapt dynamically. The ideal software radio interoperates with any communications service in its RF (Tsurumi and Suzuki, 1999) pre-selector band and ADC bandwidth. By running a different algorithm, the software radio instantaneously reconfigures itself to the appropriate signal format. This opens interesting possibilities for expanded radio services. A future software radio might autonomously select the best transmission mode that is personal communication network, mobile cellular network, etc, send probing signals

to establish a link, explore communications protocols with the remote end and adapt to the remote signal format. It could select the mode for lowest cost, service availability or best signal quality. The software radio reconfigures itself on the fly to support the required services (Mitola, April 1993). The SDR can be used in various fields and SDR is a part of cognitive radio (Niyato and Hossain, 2008). Cognitive radio (Gandetto and Regazzoni, 2007) is used in wireless communication in which either network or wireless node changes its transmission or reception parameters to communicate efficiently avoiding interference with licensed or unlicensed users. This alteration of parameters is based on the active monitoring of several factors in the external and internal radio environment, such as radio frequency spectrum, user behavior and network state.

For the SDR, OTA (Michael et al, 2002) software downloads can provide seamless interoperability without relying on any additional equipment or spectral assets. By using OTA software downloads, arriving first responders can download the interoperability parameters and immediately gain access to the host radio system. SDR is also expected to solve the compatibility problem among various mobile communication standards so that people can use the same device for different mobile environment.

6.2 M-Ary PSK Digital Modulation

In digital communication MPSK (Hao et al, 2005) is very popular.

$$\theta_i = \frac{2\Pi i}{M} + \varphi$$

where $i = 0,1,2,\ldots,$ M -1, $M = 2^n$ And φ is the initial phase. Here, we are going to consider rectangle envelop MPSK, modulated signal time-domain is expressed as:

$$Z_{MPSK}(t) = \left[\sum_n \sqrt{\frac{2E_s}{T_s}} rect(t - nT_s) \right] \cos[\omega_c t + \theta(n)] \qquad (6.1)$$

Here, T_s is the symbol duration (Harris and Rice, 2001), E_s is the unit symbol's signal energy, $\theta(n)$ is the carrier phase at $t = nT_s$ and $rect$ is rectangle function. Value is given as:-

$$rect(t) = \begin{cases} 1, & 0 \le t \le Ts \\ 0, & \text{Others} \end{cases}$$

$\theta(n) \in \{\theta_i\}$ Where $i = 0, 1, 2, \ldots, M$ -1 Derived from formula (6.1). If initial phase $\varphi = 0$, then

$$Z_{MPSK}(t) = \left[\sum_n a_n \, rect(t - nT_s)\right] \cos \omega_c t - \left[\sum_n b_n \, rect(t - nT_s)\right] \sin \omega_c t \qquad (6.2)$$

where

$$a_n = \sqrt{\frac{2E_s}{T_s}} \cos \theta(n)$$

$$b_n = \sqrt{\frac{2E_s}{T_s}} \sin \theta(n)$$

From (6.2), we can say that MPSK signal is orthogonal.

6.3 Results and Discussion

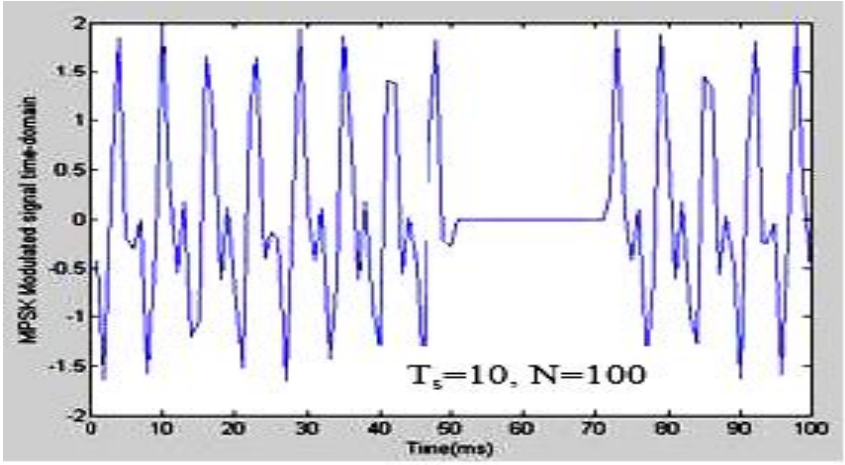


Figure 6.1 MPSK modulation.

When T_s equals to 10 and N equals to 100 our graph have greater time interval, where N is the number of terms, as shown in Figure 6.1.

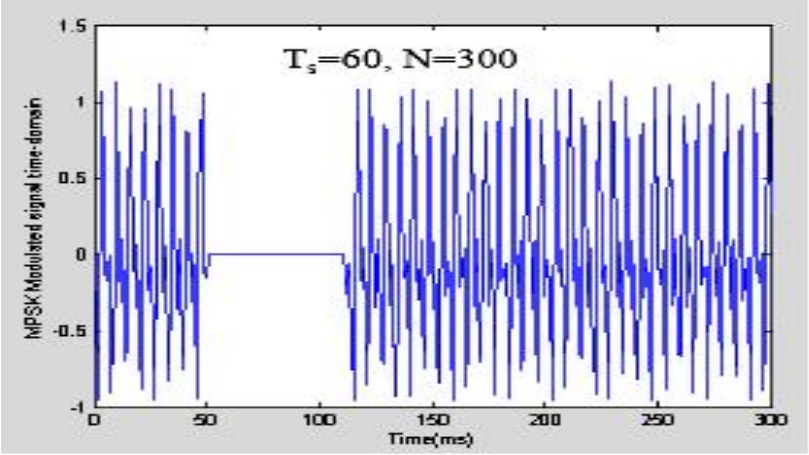


Figure 6.2 Left shifting of the gap and compression of signal.

When we increase T_s to 60 and N to 300 our graph compresses and tends to orthogonal. We will get close to ideal (orthogonal) if we will increase T_s and N as shown in Figure 6.2.

6.4 Conclusion

With the use of SDR, we can change the parameter of Ad-hoc network by using M-ary PSK modulation technique. Just by changing software, we achieved the desired output. Hence it reduces the task to a great extent. In continuous phase rate modulation, we can identify them for each phase rate properties. These can be implemented by the software radio. These are involved in many specific problems such as differential encoding MPSK and filter before modulation. We need to differentiate them according to their new properties as phase. These concepts will be used to develop adaptive software for various applications.

CHAPTER-7

CONCLUSION AND FUTURE SCOPE

Software radio is one of the key enabling technologies for the future wireless and multimedia communication systems. It enhances flexibility and lowers the costs of constructing and operating wireless infrastructure and provides a vast untapped potential to personalize services. By enabling digital conversion closer to the antenna, software radio facilitates the exploitation of new techniques in wireless communications ranging from smart antennas to adaptive power management to advanced digital signal processing. In this thesis, using DSP a novel linearizing technique is proposed for pulse shaping. The linearizing scheme is simple to implement using commercially available DSP processors. It is clear that the processed pulse-shape is closer to the ideal source pulse and the information content is not lost.

Digital beam forming can meet the challenges of increasing spectral efficiency and improving wireless communication system performance by significantly increasing the reception and transmission ranges and reducing the probability of interception of secure transmission. In digital beamformer, we have shown a new technique of implementing a digital beamformer which produces exceptionally narrow footprint. In the frequency allocation, we have targeted the problem of SDR transmission security and portability by devising a method for authentication for usage through the use of smart card technology with integrated flash memory. The model proposed shows how matching digitized frequencies and authenticating users pave the way for a secure transmission and implementing the software using smart cards that makes software piracy an impossible task. The card is overcoming any kind of brute force attack by giving a limited number of chances of trial for entering user information after which the card can be blocked and the user on whose name the card is registered can be blocked. A lot of research on software radio issues concerning future commercial and military multi-band, multi-mode applications is going on all over the world. Since dynamic range requirement in multi-band, multi-mode receivers may be very large compared to conventional designs in RF it is an important research

issue. One of the major problems for developing software radios is the incompatibility of development tools, which causes extra delay and work to be done before designers can demonstrate and evaluate overall performance of the system. The complexity of the RF stage of software radio is increased greatly when adaptive antennas are taken into use. In this case further studies for intelligent transceiver architectures must be made. Our hardware is accepting the radio signal by omni-antenna and then it is transferred to DSP Kit. We processed the signal by software called code-composer and did up to four time overlapping for security purpose and got the original signal back again by reversing the process. The entire spectrum takes only 4 ms to measure. The limitation of this measurement is its resolution. Because the time record is only 4 ms long, the frequency resolution is only 250 Hz. Suppose the signal has a frequency component at 260 Hz. The FFT spectrum will detect this signal but place part of it in the 250 Hz point and part in the 500 Hz point. One way to measure the signal accurately is to lengthen the time record and change the span of the spectrum.

With the use of SDR, we can change the parameter of Ad-hoc network by using M-ary PSK modulation technique. Just by changing software, we achieve the desired output. Hence it reduces the task to a great extent. In continuous phase rate modulation, we can identify them for each phase rate properties. These can be implemented by software radio. These are involved in many specific problems such as differential encoding MPSK and filter before modulation. We need to differentiate them according to their new properties as phase. These concepts will be used to develop adaptive software using various applications.

The current frontier for software radio research is focused on what is referred to as “Cognitive Radio”. The basic idea is to make radio receivers and transmitters more intelligent via software, including artificial intelligence (AI) and adaptive so that they can respond to changes in their local environment. These may include adapting to changing interference or congestion conditions, or adapting to facilitate interoperability among diverse devices, or adapting to accommodate the requirements of changing applications e.g., from wireless email to voice to video. Cognitive radios would be self-configuring. The increased adaptability to local conditions would greatly expand the range of services that could be offered and the range of congestion

management that is to address spectrum scarcity concerns strategies that might be employed.

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