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TEST -1 EXAMINATIONS-2022

B.Tech-VI Semester (ECE)

COURSE CODE: 18B11EC612 MAX. MARKS: 15

COURSE NAME: VLSI TECHNOLOGY

COURSE CREDITS: 4 MAX. TIME: 1 Hour

***Note:** All questions are compulsory. Marks are indicated against each question in square brackets.*

Q1. (a) What are the differences between semi-custom and full-custom design? [1.5]

(b) What do you understand by concepts of regularity, modularity and locality? [1.5]

Q2. VLSI design flow is explained by Y-chart, explain it. Write the differences between functional yield and parametric yield. [03]

Q3. Discuss the structure and operation of MOSFET. Develop the expression for maximum depletion region depth. [03]

Q4. Consider the following n-channel MOSFET process:

Substrate doping $N_A = 1.45*10^{15}$ cm^{-3}, polysilicon gate doping density $N_D = 10^{20}$ cm^{-3}, gate oxide thickness $t_{ox} = 500$ Å and oxide-interface charge density $N_{OX} = 10^{10}$ cm^{-2}.

Use $\varepsilon_{si} = 11.7\varepsilon_0$ and $\varepsilon_{ox} = 3.97\varepsilon_0$ for the dielectric coefficients of the silicon and silicon–dioxide, respectively. The intrinsic concentration of silicon is $1.45*10^{10}$ cm^{-3}.

(a) Calculate the threshold voltage V_{T0} for $V_{SB} = 0$ V. [02]

(b) Determine the type and the amount of channel ion implantation which are necessary to achieve a threshold voltage of $V_{T0} = 1$ V. [01]

Q5. An enhancement-type nMOS transistor has the following parameters:

$V_{T0} = 0.8$ V, $\gamma = 0.2$ V$^{1/2}$, $\lambda = 0.05$ V^{-1}, $|2\varphi_F| = 0.58$ V, $\mu_n C_{ox} = 20$ μA/V^2

When the transistor is biased with $V_G = 2.8$ V, $V_D = 5$ V, $V_S = 1$ V, and $V_B = 0$ V, the drain current is $I_D = 0.24$ mA. Determine W/L. [03]