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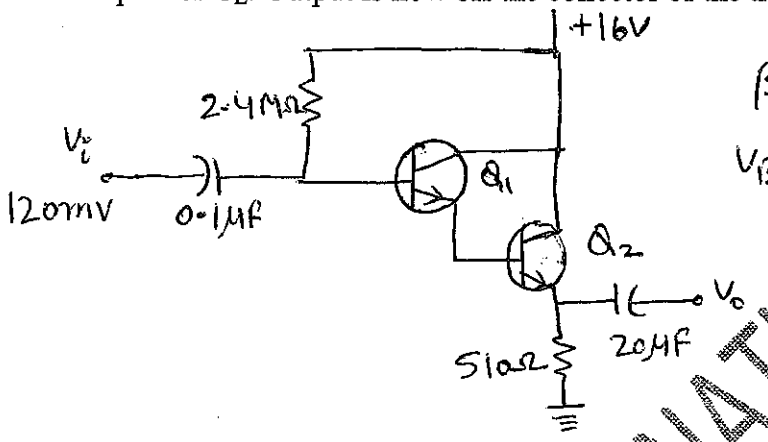
JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT
TEST -2 EXAMINATION- October 2017
B.Tech (ECE) 3rd Semester

COURSE CODE: 10B11EC312 MAX. MARKS: **25**
COURSE NAME: Analog Electronics
COURSE CREDITS: **4** MAX. TIME: **1.5 Hrs**

Note: All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means.

Q1- For the given Darlington transistor draw the ac equivalent circuit, r_e model and Calculate the voltage gain. Repeat the problem if a resistor R_c= 200KΩ is added along with a bypass capacitor C_E. Output is now off the collector of the transistor. In both the cases ignore r_o. **[6]**



Q2- (a) Draw the neat circuit diagram of Emitter follower and show that in emitter follower A_V=1.Ignore r_o. **[4]**

(b) Given h_{ie} = 2.2KΩ, h_{fe} = 100, h_{re} = 4×10^{-4}, and h_{oe} = 25μS, draw the following:

i. Common Emitter hybrid equivalent model.
ii. Common Emitter r_e equivalent model
iii. Common base hybrid equivalent model
iv. Common base r_e equivalent model **[2]**

Q3- For voltage divider bias circuit with bypass capacitor C_E, prove that $A_{VNL} > A_{VL} > A_{VS}$. Ignore r_o. **[6]**

Q4- For the given cascade system with two identical stages, determine:

a. The loaded voltage of each stage.
b. The total voltage gain of the system (A_{VS})
c. The loaded current gain of each stage.
d. The total current gain of the system
e. How Z_i is affected by the second stage and R_L?
f. How Z_o is affected by the first stage and R_s
g. The phase relationship between V_o and V_i. **[7]**