Mr. Munish Sood

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT
TEST –II EXAMINATION- Oct 2018
B.Tech. III Semester (ECE)

COURSE CODE: 10B11EC312 MAX. MARKS: 25
COURSE NAME: Analog Electronics
COURSE CREDITS: 4 MAX. TIME: 1 Hr 30 Min

Note: *All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means.*

Q1) For the network of Fig.1 determine r_e, V_B, V_C, Z_i and A_{VNL}. **(5)**

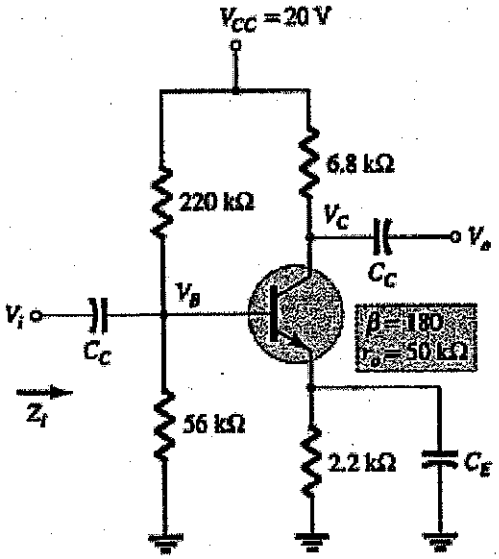


Fig.1

Q2) Calculate the voltage gain of each stage and the overall ac voltage gain for the BJT cascade amplifier circuit of Fig.2. **(5)**

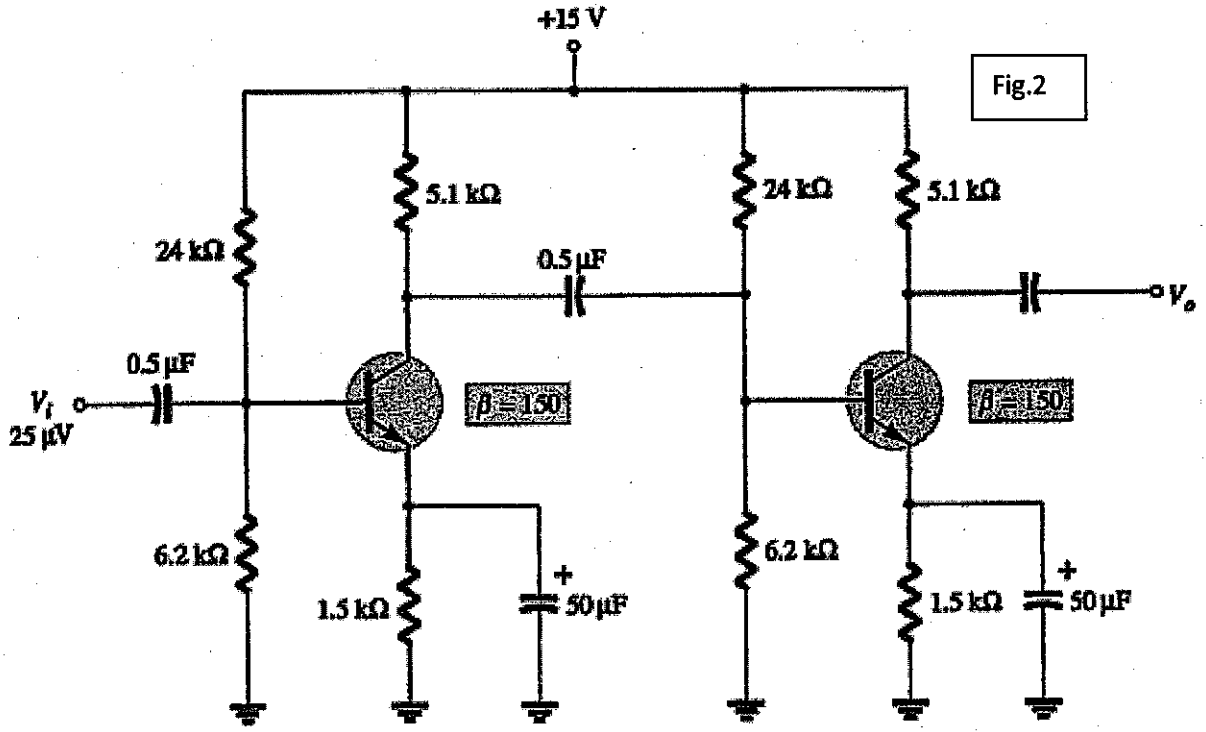


Fig.2

Q3) Determine Z_i, Z_o and A_v for the network of Fig.3 if $I_{DSS} = 10mA$, $V_P = -4V$, and $r_d = 40\ K\Omega$. **(5)**

Fig.3

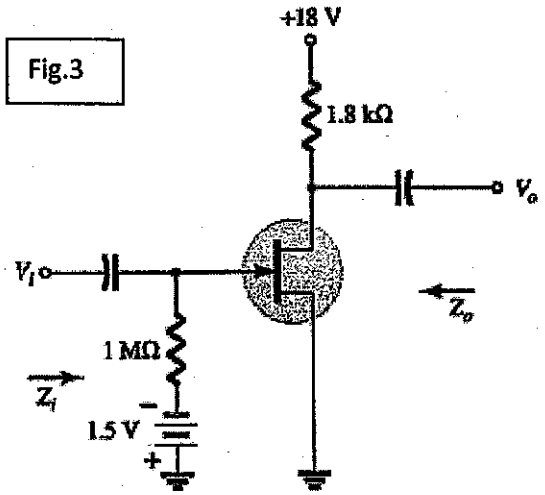
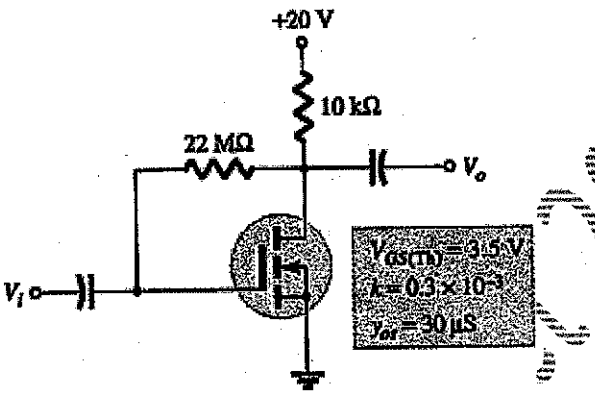


Fig.4



Q4) Determine V_o for the network of Fig.4 if $V_i = 4$ mV, $I_{D\,(on)} = 4$ mA and $V_{GS(on)} = 7V$. **(5)**

Q5) For the self Bias JFET network of Fig. 5. Determine $A_{V(NL)}$, Z_I and Z_O and A_{VS} (voltage gain with source resistance and load resistance) **(5)**

Fig.5