Munish Sud.

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT
TEST -1 EXAMINATION- Sep 2018
B.Tech III Semester (ECE)

COURSE CODE: 10B11EC312 MAX. MARKS:15
COURSE NAME: Analog Electronics
COURSE CREDITS: 4 MAX. TIME: One Hr

Note: *All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means.*

Q1) Given that I_{CQ} = 2mA and V_{CEQ} = 10 V. Determine R_1 and R_C for the network of Fig. 1. (3)

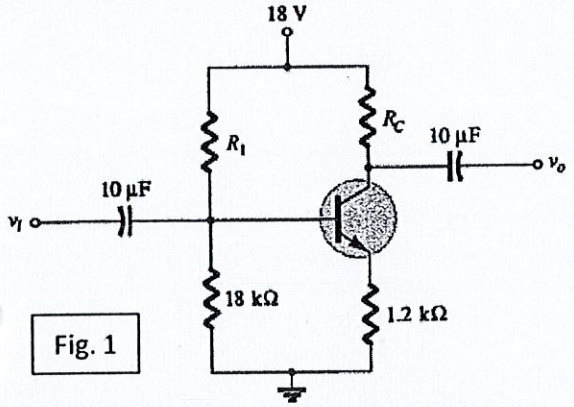


Fig. 1

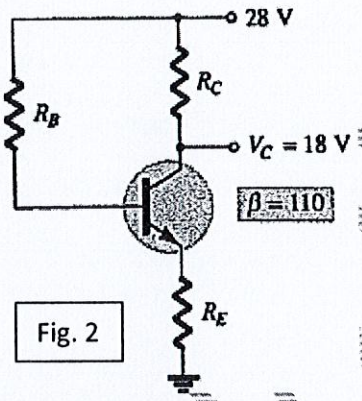


Fig. 2

Q2) The emitter bias configuration of Fig. 2 has the following specification. I_{CQ} = ½ I_{Csat}, I_{Csat} = 8mA, V_C = 18 V and β = 110. Determine R_E, R_C and R_B. (3)

Q3) For the collector to base feedback configuration given in the following Fig.3. compute the expression for Z_i, Z_o and A_v (3)

Fig. 3

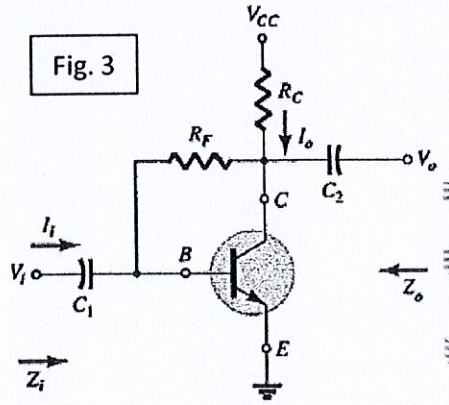
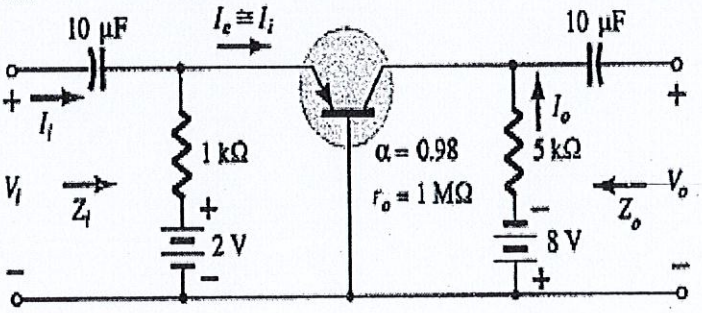


Fig. 4



Q4) For the network of Fig. 4 determine re, Z_i, Z_o and A_v (3)

Q5) For the voltage divider bias configuration given in Fig. 5 determine S(I_{CO}). (3)

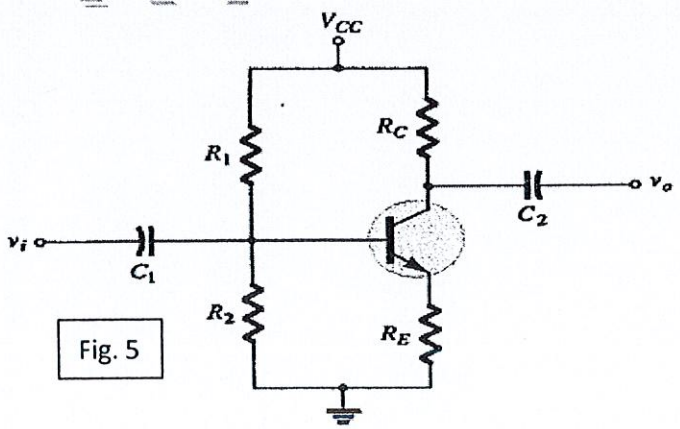


Fig. 5