COURSE CODE: **10B11CI401**   MAX. MARKS: **35**
COURSE NAME: **MICROPROCESSORS AND CONTROLLERS**
COURSE CREDITS: **4**   MAX. TIME: **2 Hrs**

Note: *All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means. Missing data, if any, can be appropriately assumed.*

1(a). What is an interrupt vector? How many different interrupt vectors are there for the 8086 processor and what do they contain?   [CO4, 2M]

(b) What are INTO and INT 3 ? Briefly describe a situation where it is used?   [CO4, 1M]

(c) Highlight the differences between software interrupt and the CALL instruction.   [CO4, 2M]

2. With suitable timing diagrams describe briefly the burst mode and cycle stealing operation of DMA. Which is more efficient and why?   [CO3, 5M]

3. Illustrate with suitable sketch, various registers available in Pentium processor for the MMX and SSE instruction set. Describe how MMX and SSE technology can enhance the performance of the Pentium processor.   [CO5, 5M]

4. What are the different addressing modes available for 8051 microcontroller? With a suitable sketch explain the architecture of 8051 microcontroller.   [CO6, 5M]

5. What is the word length of registers available in 8087 math coprocessor? How do they function? With a neat sketch explain the architecture of 8087 math coprocessor.   [CO3, 5M]

6. What are the program invisible registers available in a Pentium processor? Explain the working method of the protected mode memory in Pentium processor using descriptors.   [CO5, 5M]

7. An 8086 based system uses 16550 UART to read the data from a temperature sensor, which is connected to the system by using an RS-232-C serial communication channel. The temperature sensor will respond to a command "TEMP?" in ASCII string format by transmitting the current temperature as a 3 digit ASCII coded decimal number. Write a program to initialize the 16550 and read the temperature from the sensor and store at memory location starting at 2000:0100H. Assume a clock frequency of 18.432MHz, 2400 baud rate, 8 data bits, 2 stop bits and even parity. The FIFO buffer and Line Control Register are addressed at 30H and 33H respectively. The format of Line Control Register and FIFO control registers and Status Register are given below.   [CO3, 5M]

DL	SB	ST	P	PE	S	L1	L0

Enable divisor latch
Send break, 0 = off
Stick bit, 0 = stick parity off
Parity type, 0 odd.

Data length:
00 = 5 bits, ... 11 = 8 bits.
Stop bits: 0 = 1, 1 = 1.5/2
Parity enable

RT1	RT0	0	0	DMA	XMIT RST	REVC RST	EN

Receiver trigger level
1/4/8/14 byte in FIFO
DMA mode control

FIFO Enable
Reset receiver FIFO
Reset transmitter FIFO

ER	TE	TH	BI	FE	PE	OE	DR

Error in FIFO if 1
Transmitter empty if 1
Transmitter holding register
Break indicator: 1 = received

Data ready, 0: no data
Overrun Error if 1
Parity error if 1
Framing error if 1