Pragya Gupta

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST 2 EXAMINATION - OCTOBER 2018

B.Tech 5TH Semester (ECE)

COURSE CODE: 17B11EC511 MAX. MARKS: 25

COURSE NAME: Linear Integrated Circuits

COURSE CREDITS: 04 MAX. TIME: 1.5 HRS

Note: *All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means. Marks are indicated against each question in square brackets.*

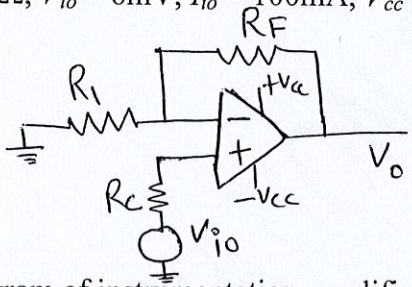
Q1. For a non-inverting amplifier, determine the – **[2+1+2]**

a) Maximum possible output offset voltage V_{oo} due to input offset voltage V_{io} and input offset current I_{io}.

b) What value of compensating resistance R_c is needed to reduce the effect of input offset current.

c) What is the effect of input offset voltage and input offset current on the output voltage V_o

$R_1 = 100\Omega$, $R_F = 10K\Omega$, $V_{io} = 6mV$, $I_{io} = 100mA$, $V_{cc} = \pm 15V$, $I_B = 500nA$, $V_{in} = 10mV$



Q2. Draw the circuit diagram of instrumentation amplifier and show that under unbalanced condition- **[3+2]**

$$V_{ab} = -\frac{\Delta R V_{dc}}{2(2R+\Delta R)} \quad \text{and} \quad V_0 = \frac{\Delta R R_f V_{dc}}{4RR_1}$$

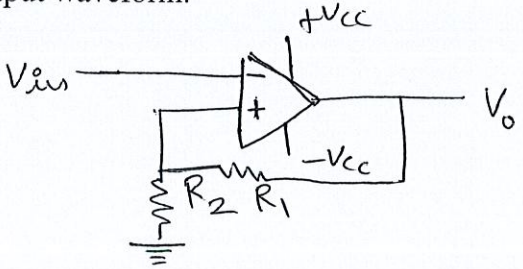
Assume that under unbalanced condition change in the transducer resistance (R_T) is ΔR. Also assume that $R_A = R_B = R_C = R_T = R$.

Q3. For the positive clamper circuit, draw the output wave form, if V_{in} is 500mV peak sine wave at 100Hz and $V_{ref} = +200mV$. **[5]**

Q4. In the give circuit $R_1 = 68\ k\Omega$, $R_2 = 150\Omega$, Vin = 500mV P-P sine wave and $V_{sat} = \pm 14V$

a) Determine the threshold voltages $\pm V_T$

b) Draw the output waveform. **[2+5]**



Q5. Design a fourth order low pass Butterworth filter at a cut off frequency of 1kHz using IC741. Also draw the schematic diagram with component values. **[5]**