JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -1 EXAMINATION- 2026

B.Tech- VI Semester (ECE)

COURSE CODE (CREDITS): 18B11EC612 (4) MAX. MARKS: 15

COURSE NAME: VLSI TECHNOLOGY

COURSE INSTRUCTORS: Dr. Shruti Jain MAX. TIME: 1 Hour

Note: *(a) All questions are compulsory.*
(b) The candidate is allowed to make Suitable numeric assumptions wherever required for solving problems
(c) Use of calculators is allowed

Q.No	Question	CO	Marks
Q1	i. What is the effect of substrate bias on the linear current of *p*-MOS transistor? State the condition also. ii. Sita is working on threshold voltage. She comes to know that total voltage comprises different parts. Help her in explaining those parts. (Write all formulas). iii. What is the Fermi potential for depletion mode *n*-substrate and enhancement mode *p*- substrate? iv. Help Shyam in explaining that depth of depletion region is a function of Fermi potential. v. Show diagrammatically length of source, and oxide thickness of *n*-MOS transistor.	CO 1	5
Q2	i. The drain of an n – channel MOSFET is shorted to the gate. The threshold voltage (V_T) of MOSFET is 1 V. If the drain current (I_D) is 1 mA for V_{GS} = 2 V, then evaluate the drain current for V_{GS} = 3V. Is there any effect of scaling if factor is 2? ii. An nMOS transistor with $\lambda = 0.01V^{-1}$ is operated at a dc current I_D = 1 mA. If the channel length is doubled, find the new values of λ, V_A, I_D,and r_o when V_{GS} and V_{DS} are fixed.	CO 2	2.5 + 2.5
Q3	Consider following parameters for Depletion *n*-channel MOSFET: electron mobility = 500 cm^2/ V.sec, aspect ratio = 1.0, gate oxide thickness = 345Å, $\lvert 2\phi_f \rvert$ = 0.84V and substrate bias coefficient = 2.3. Some laboratory measurements results of terminal behavior of this device are shown in table 1. Using the data in the table, find the missing value of the gate voltage in the last entry. Show all of the details of your calculation.	CO 1	5

I_{DS} (µA)	V_D	V_S	V_B	V_G
50	3V	0	0	0
40	5V	3V	0	?

40