JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -1 EXAMINATION- 2026

B. Tech.-IV Semester (EE (VLSI Design & Technology))

COURSE CODE (CREDITS): 25B11EC415 (3) MAX. MARKS: 15

COURSE NAME: INTRODUCTION TO MICROFABRICATION TECHNOLOGY

COURSE INSTRUCTOR: Dr. Harsh Sohal MAX. TIME: 1 Hour

Note: *(a) All questions are compulsory.*

(b) The candidate is allowed to make Suitable numeric assumptions wherever required for solving problems

(c) Use of calculators is allowed

Q.No.	Question	CO	Marks
Q1	Discuss various levels of abstractions in building an IC with the help of a block diagram.	1	2
Q2	Explain the following with reference to VLSI Technology : (a) Moore's Law (b) the concept of planar technology	1	2
Q3	Compare the Constant Voltage scaling with Constant Electric Field scaling. The practical scaling approach called as 'Denard Scaling' is an extension of which of the scaling type? Discuss.	1	2
Q4	You are given a wafer of the size of 30 cm, die size of 2.5 cm^2, with 1 defects/cm^2; α (the measure of manufacturing process complexity) =3. Cost of the wafer is INR 200,000. Calculate: (i) dies per wafer (ii) die yield (iii) cost of one die.	2	1+1+2
Q5	(a) What is the significance difference between the construction of an enhancement-type MOSFET and a depletion-type MOSFET? Draw the cross sections of both. (b) For an E-MOSFET, given $k = 0.4 \times 10^{-3}$ A/V^2 and I_D(on) = 3 mA with V_{GS}(on) = 4V, determine V_T . (c) Define Pinch Off Voltage in a JFET.	1	2+2+1

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