JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -1 EXAMINATION- 2026

B. Tech.-IV Semester (CSE/IT/BT/ECE/CE)

COURSE CODE (CREDITS): 18B1WEC744 (3) MAX. MARKS: 15

COURSE NAME: FPGA based Instrumentation System Design

COURSE INSTRUCTOR: Dr. Harsh Sohal MAX. TIME: 1 Hour

Note: *(a) All questions are compulsory.*

(b) The candidate is allowed to make Suitable numeric assumptions wherever required for solving problems

(c) Use of calculators is not allowed

Q.No.	**Question**	**CO**	**Marks**
Q1.	(a) Classify various FPGAs on the basis of user programmable technology used. Explain the SRAM based programmability technique with suitable diagrams. (b) Explain the architecture of PAL, PLA.	1	3+2
Q2.	You are an R&D engineer working for Philips in the development of a new hardware efficient MRI Machine as early as possible. Which among the FPGA and ASIC shall you choose? Explain the reasons for your choice while giving a detailed comparison of the two.	1	3
Q3.	(a) Why FPGA platform is said to provide flexibility over PDSPs? Discuss with an example of FIR filter implementation. Also show fully parallel, fully serial and semi parallel implementation block diagrams. (b) Assuming one Multiply accumulate operation (MAC) operation takes one clock cycle, how many clock cycles will be required to get the first output from a 31 tap filter implemented in a fully serial implementation in an FPGA?	1	3 +1
Q4.	What are different modeling styles in verilog HDL? Write verilog code for implementing a Half Adder circuit using: a) gate level modeling style b) Data flow modeling style	2	3

117