

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

Supplementary Examination- 2026

B.Tech- V Semester (CSE/IT)

COURSE CODE(CREDITS): 18B17CI514 (3)

MAX. MARKS: 75

COURSE NAME: Computer Organization and Architecture

COURSE INSTRUCTORS: NTS\*, PMI, KTS, SKS

MAX. TIME: 2 Hours

**Note:** (a) All questions are compulsory.

(b) The candidate is allowed to make Suitable numeric assumptions wherever required for solving problems

Q.No	Question	CO	Marks
Q1	A processor runs at a clock rate of 3 GHz. The average CPI for a program is 1.8 and the program executes $5 \times 10^9$ instructions. (a) Calculate the CPU execution time. (b) If the CPI is reduced to 1.5, find the percentage improvement in performance.	2	8
Q2	(a) Represent the decimal number -18.375 in IEEE-754 single precision floating point format. (b) Perform floating-point addition for the numbers 5.25 and -2.75 using normalized representation.	2	10
Q3	Explain instruction pipelining. Discuss data, control, and structural hazards and the techniques used to resolve them.	5	8
Q4	A cache memory has the following parameters: Cache size = 64 KB Block size = 64 bytes Main memory size = 1 GB Calculate: (a) Number of cache lines (b) Number of bits in tag, index, and offset for a direct-mapped cache	3	8
Q5	Compare Program-controlled I/O, Interrupt-controlled I/O, and DMA-controlled I/O. Explain their advantages and limitations.	4	8
Q6	A pipeline has 5 stages with a clock cycle time of 1 ns. (a) How long does it take to execute 100 instructions without pipelining? (b) How long does it take with pipelining (ignore hazards)? (c) Calculate the speedup achieved.	5	8
Q7	A system uses a write-back cache with the following parameters: <ul style="list-style-type: none"> <li>Cache hit ratio = 0.9</li> <li>Cache access time = 1 ns</li> <li>Main memory access time = 60 ns</li> <li>Write-back occurs for 25% of cache block replacements</li> <li>Write-back penalty = 40 ns</li> </ul>	3	8

	Calculate the Average Memory Access Time (AMAT).		
Q8	<p>A 5-stage pipeline has a clock cycle of 1.2 ns. Due to data hazards, 20% of instructions incur a stall of 1 cycle.</p> <p>(a) Compute the effective CPI (b) Calculate the execution time for 200 instructions.</p>	5	8
Q9	<p>A 3-block cache initially empty receives the following memory reference string:</p> <p>1, 2, 3, 4, 1, 2, 5, 1, 2, 3, 4, 5</p> <p>(a) Calculate cache hits and misses using LFU replacement (b) Calculate cache hits and misses using LRU replacement (c) Calculate cache hits and misses using MFU replacement</p>	3	9