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**JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT**

Supplementary Examination- 2026

B.Tech-I Semester (CSE (all branches)/IT/ECE/ECS/EEVLSI/CE)

COURSE CODE(CREDITS) : 25B11EC111

COURSE NAME: BASIC ELECTRONICS

COURSE INSTRUCTORS: Prof. Rajiv Kumar, Prof. Shruti Jain, Dr. Harsh Sohal, Dr. Shweta Pandit, Dr. Salman Raju, Dr. Nishant Jain, Dr. Alok Kumar, Lt. Pragya Gupta.

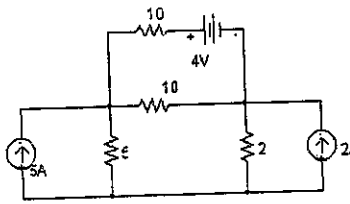
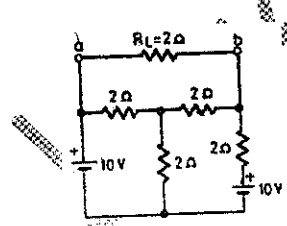
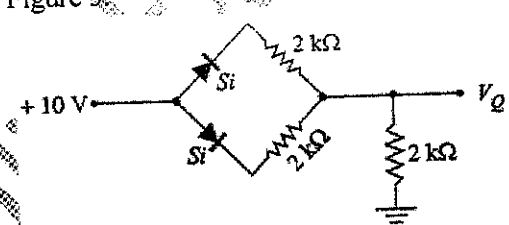
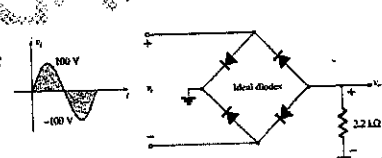
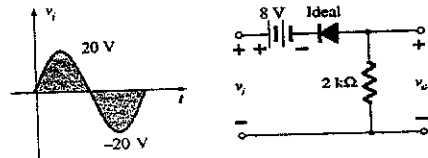
MAX. MARKS: 75

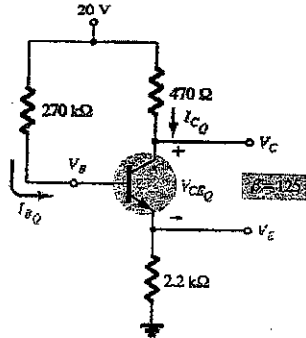
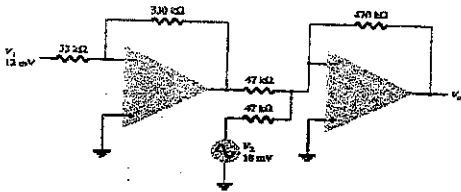
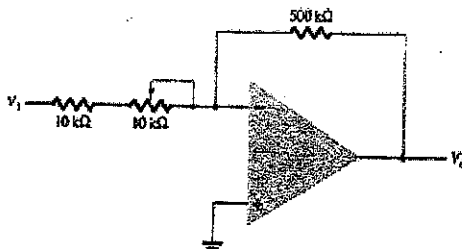
MAX. TIME: 2 Hours

Note: (a) All questions are compulsory.

(b) The candidate is allowed to make Suitable numeric assumptions wherever required for solving problems

(c) Calculator(non-programmable) is allowed.

Q.No	Question	CO	Marks
Q1	<p>i. Using nodal analysis find voltages at all the nodes and current flowing in <math>2\Omega</math> resistors as shown in Fig 1.</p>  <p style="text-align: center;">Fig 1</p>  <p style="text-align: center;">Fig 2</p> <p>ii. Find the current in <math>R_L</math> in the circuit of Fig. 2 by using Thevenin's theorem.</p>	1	5 + 5
Q2	<p>i. Determine the thermal voltage for a diode at a temperature of <math>25^\circ\text{C}</math>. For the same diode find the diode current if <math>I_s = 30\text{nA}</math>, <math>n = 2</math> and the applied bias voltage is <math>0.4\text{V}</math>.</p> <p>ii. Find <math>V_Q</math> in the Figure 3.</p>  <p style="text-align: center;">Fig 3</p>	2	5 + 5
Q3	<p>With proper explanation, for the given input waveforms, determine the output waveform, <math>V_o</math> for the circuit shown in Fig 4 (a) and Fig 4 (b).</p>  <p style="text-align: center;">Fig 4 (a)</p>  <p style="text-align: center;">Fig 4 (b)</p>	2	5 + 5

Q4	<p>i. With reference to Bipolar Junction Transistors (BJTs), discuss whether the nature of majority and minority charge carriers changes when the base material is changed from silicon to germanium. Justify your answer.</p> <p>ii. In a Common-Base (CB) configuration of a BJT, explain how the DC current gain (<math>\alpha_{DC}</math>) is defined. For the operating conditions : <math>I_E = 2.8 \text{ mA}</math>, <math>I_C = 2.79 \text{ mA}</math>, and <math>I_{CBO} = 0.1 \mu\text{A}</math>, calculate the DC current gain (<math>\alpha_{DC}</math>).</p>	4	5 + 5
Q5	<p>i. What is the need of biasing a transistor? How do you differentiate between an <math>n</math>-<math>p</math>-<math>n</math> transistors biasing from <math>p</math>-<math>n</math>-<math>p</math> transistor biasing? Draw any biasing circuit of your choice to indicate the polarities of voltages and current directions for a <math>p</math>-<math>n</math>-<math>p</math> and an <math>n</math>-<math>p</math>-<math>n</math> transistor.</p>  <p>Fig 5</p> <p>ii. For the circuit shown in Fig 5, determine <math>V_{CE}</math> and <math>V_E</math>. What is the effect of <math>\beta</math> on <math>I_B</math> if it is changed from 125 to 75? Does a change in <math>\beta</math> alter the operating/quiescent point or not?</p>	4	5 + 5
Q6	<p>i. What are the significant differences between the construction of JFET and MOSFET? Explain.</p> <p>ii. Sketch the transfer and drain characteristics of an <math>n</math>-channel enhancement-type MOSFET if <math>V_T = 2.12 \text{ V}</math> and <math>k = 0.4 \times 10^{-3} \text{ A/V}^2</math>.</p>	4	5 + 5
Q7	<p>i. Determine the output voltage for the circuit shown in following Fig 6?</p>  <p>ii. What is the range of the voltage-gain adjustment in the circuit given Fig 7 shown below?</p> 	5	5 + 5
Q8	<p>i. What is CMRR? How does it affect the noise in an Operational Amplifier?</p> <p>ii. Determine the output voltage of an op-amp for input voltages of <math>V_{i1} = 150 \text{ mV}</math> and <math>V_{i2} = 140 \text{ mV}</math>. The amplifier has a differential gain of <math>A_d = 4000</math> and the value of CMRR = 100.</p>	5	2 + 3