JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -3 EXAMINATION- 2025

B.Tech-V Semester (CSE/IT/ECE/CE/BT/BI)

COURSE CODE (CREDITS):18B11CI514 (3) MAX. MARKS: 35

COURSE NAME: Computer Organization and Architecture

COURSE INSTRUCTORS: NTS*, PMI, KTS, SKS MAX. TIME: 2 Hours

Note: *(a) All questions are compulsory.*

(b) The candidate is allowed to make Suitable numeric assumptions wherever required for solving problems

Q.No	Question	CO	Marks
Q1	An instruction pipeline consist of following five stages: IF = Instruction Fetch, ID = Instruction Decode, EX = Execute, MA = Memory Access, WB = Write Back. Consider the following code: LOAD R_1, [1000] $R_1 \leftarrow$ Memory[1000] LOAD R_3, 4(R_2) $R_3 \leftarrow$ Memory[R_2 + 4] MUL R_4, R_1, R_3 $R_4 \leftarrow R_1 \times R_3$ DIV R_5, R_1, R_3 $R_5 \leftarrow R_1 / R_4$ SUB R_6, R_4, R_5 $R_6 \leftarrow R_4 - R_5$ Assume that each stage takes one clock cycle for all instructions. Calculate the number of clock cycles needed to execute the code: (i) Using Operand Forwarding (ii) Without operand Forwarding	5	7
Q2	Consider an instruction pipeline with five stages without any branch prediction: Fetch Instruction (FI), Decode Instruction (DI), Fetch Operand (FO), Execute Instruction (EI) and Write Operand (WO). The stage delays for FI, DI, FO, EI and WO are 5 ns, 7 ns, 10 ns, 8 ns and 6 ns, respectively. There are intermediate storage buffers after each stage and the delay of each buffer is 1 ns. A program consisting of 12 instructions I1, I2, I3, …, I12 is executed in this pipelined processor. Instruction I4 is the only branch instruction and its branch target is I9. If the branch is taken during the execution of this program, calculate the time (in ns) needed to complete program execution. Show steps clearly involved in calculation.	5	7
Q3	(A) A processor uses a 5-stage pipeline with each stage taking 40 ns. Do the following. (i) Compute the pipeline latency. (ii) Calculate the execution time for 12 instructions under ideal conditions. (iii) Compare the speedup with a non-pipelined processor that takes	6	4 + 3

	200 ns per instruction. (B) Explain principle of locality and its types in detail.		
Q4	What is a DMA controller? With the help of a neat block diagram, describe DMA-controlled I/O. Discuss how DMA achieves higher performance than interrupt-driven I/O.	4	7
Q5	An 8KB direct-mapped write-back cache is organized as multiple blocks, each of size 32-bytes. The processor generates 32-bit addresses. The cache controller maintains the tag information for each cache block comprising of the following. 1 Valid bit 1 Modified bit As many bits as the minimum needed to identify the memory block mapped in the cache. What is the total size of memory needed at the cache controller to store meta-data (tags) for the cache?	4	7