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JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -3 EXAMINATION- May 2018

B.Tech VI Semester

COURSE CODE: 10B11EC612 MAX. MARKS: 35

COURSE NAME: VLSI TECHNOLOGY AND APPLICATIONS

COURSE CREDITS: 04 MAX. TIME: 2 Hrs

Note: *All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means.*

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1. **[CO1, CO2, CO3, CO4, CO5][1 * 10 =10]**

I. Show analytically by using equations how the gate capacitance is affected in terms of scaling factor S using full scaling method.

II. Specify the colors for *n*-diffusion, metal 1 layer, polysilicon and demarcation line in stick diagram.

III. Find the region of operation for the MOSFET working with following parameters: V_G = -1V, V_S = 2V, V_D = -3V, V_{th} = -1.5V?

IV. In general, *p*-MOS in series implement a _____gate. How many *n*-MOS transistors are in logic diagram of NAND 3 gate?

V. Does the substrate bias effect, affect CMOS circuits? How.

VI. What is the formula for C_{GD} and C_{GB} in saturation region for oxide related capacitance? Assume overlap length.

VII. If V_{OH} = 4.5V, V_{OL} = 0.3V, $\gamma = 0.38V^{1/2}$ and $|2\phi_f| = 0.6V$. Find the threshold voltage for load assuming this value is used in calculation of V_{IL}. Assume V_{TO} = 0.8V .

VIII. Give the formula for voltage equivalence factor (K_{eq}) and zero bias capacitance (C_{J0}).

IX. Find i as a function of v for the circuit shown in Fig 1 for linear and saturation region. Neglect the effect of λ on v_{DS} - i_D in the saturation region.

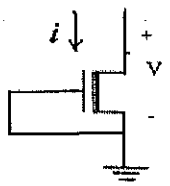

Fig 1

X. Assuming linear load, draw the logic diagram for $\overline{AB+CD}$.

2. A NOR3 gate uses identical *n*-MOS and *p*-MOS with an aspect ratio of 4 for each MOS. The *n*-MOS process trans-conductance is 120μA/V^2, and the threshold voltage of 0.55V. A power supply of 5V is chosen for the circuit. Find the value of *p*-MOS process trans-conductance needed to create a gate where the case of simultaneous switching gives the midpoint of 2.4V. Assume V_{tp} = - 0.9V. **[CO1, CO4] [5]**

3. For the CMOS inverter V_{Tn} = 0.5V, V_{Tp}= - 0.5V , k_n`= 80μA/V$^2$, $k_p$`= 40 μA/V^2 and V_{DD}= 3.3V, $(W/L)_n = (W/L)_p = 4$.

   - Find the transition points for the *p*-MOS and *n*- MOS.
   - Find v_i, when v_0 = 0.5V
   - Find v_i when v_0 = 2.8V
   - Give the conditions for Symmetric CMOS inverter.

   [CO4] [2 + 1.5 + 1.5 + 1 = 6]

4. Explain the different steps of fabrication for enhancement *n*-type IGFET. **[CO5] [5]**

5. Draw the stick diagram of the logic expression $f(A,B,C)=\overline{A(B+C)(A+B)}$ using CMOS logic. Find the equivalent CMOS inverter circuit for simultaneous switching of all input, assuming that $(W/L)_n$ = 15 for all *n*-MOS transistor and $(W/L)_p$ = 20 for all *p*-MOS transistor. **[CO5] [5]**

6. What are pass transistors? Derive *pull up to pull down* ratio if one of the inverter is fed to another inverter through a series of three pass transistors. Assume $V_{th} = 0.2V_{DD}$, V_{thdep} = - $0.6V_{DD}$ and $V_{thp} = 0.3V_{DD}$. **[CO6][1 + 3 = 4]**