Dr Shruti

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT
TEST-2 EXAMINATION- APRIL -2018
B.Tech VI Semester

COURSE CODE: 10B11EC612 MAX. MARKS: 25
COURSE NAME: VLSI TECHNOLOGY AND APPLICATIONS
COURSE CREDITS: 04 MAX. TIME: 1 HRS 30 MIN

Note: *All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means.*

1. **(CO1, CO4) [1 × 5 = 5]**

(a) How noise sensitivity is different from noise immunity?
(b) Draw and explain the high frequency model of a MOSFET.
(c) A slow circuit dissipates less power than a fast circuit. Justify.
(d) Threshold voltage of a MOSFET is -1.35V. Which all MOSFET's satisfy this specification? Draw symbols.
(e) A depletion type *n*-channel MOSFET is biased in its linear region for use as a voltage controlled resistor. Assume V_{th} = 0.5V, V_{GS} = 2V, V_{DS} = 5V, W/L = 100, $C_{ox} = 10^{-8}$ F/cm^2 and μ_n = 800cm^2/V-sec. The value of the resistance of the voltage controlled resistor (in mΩ) is______ ____________________.

2. **(CO1, CO3) [3 + 3 = 6]**

(a) Consider *n*-MOS transistor with source and body connected together. Calculate the threshold voltage (in volts) of the transistor assuming that the electron mobility is dependent of V_{GS} and V_{DS}. Given : g_m = 0.5μA/V for V_{DS} = 50mV and V_{GS} = 2V.
g_d = 8 μA/V for V_{GS} = 2V and V_{DS} = 0V.

where $$g_m = \frac{\partial I_D}{\partial V_{GS}} \text{ and } g_d = \frac{\partial I_D}{\partial V_{DS}}$$

(b) Calculate the parasitic drain capacitance for *n*-MOS transistor operating at W = 5μm, L = 0.5μm, Y = 3 μm, ϕ_0 = 0.7V, ϕ_{0sw} = 0.9V C_{sb0} = 0.86 fF/μm^2 , C_{db0} = 0.24 fF/μm^2 , C_{sbsw} = 0.24 fF/μm, C_{dbsw} = 0.24 fF/μm, m = 0.36, m_{sw} = 0.4 and reverse bias voltage 3V.

3. **(CO3) [6]**

Design Linear RC model of an *n*-channel MOS transistor having parameters : substrate doping density = 10^{16}/cm^3, polysilicon gate doping density = 2×10^{20}/cm^3, $N_{A(chanstop)} = 10^{19}$ / cm^3 ,gate oxide thickness = 50nm, oxide interface fixed charge density = 4×10^{10}/cm^2 , abrupt junction depth = 0.4μm , length of drain = 9μm, width = 4μm, length of channel = 1.5μm, drain to bulk voltage = 1.5V, gate to source voltage = 1.5V, drain to source voltage = 1.5V, threshold voltage = 0.8V, electron mobility = 650 cm^2/ V-s. Assume diffusion capacitance.

4. **(CO4) [2 × 4 = 8]**

(a) Design a resistive load inverter with R = 1 kΩ, such that V_{OL} = 1V. The enhancement type *n*MOS driver transistor has the following parameters: $\mu_n C_{ox}$ = 22 μA/V^2, V_{TO} = 1V, V_{DD} = 4.0V. Determine the required aspect ratio. Determine input low voltage parameter.

(b) Draw the VTC curve for resistive load *n*-MOS inverter. Determine the V_{OH} and V_{OL} when biased at V_{DD} = 2.5V, k'=1μA/V^2, V_{t0D}= 0.5V, $(W/L)_D$ =10, R = 2KΩ.

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