Dr Smriti.

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

MID TERM (SUMMER SEMESTER EXAMINATION) - June-2018

B.Tech.

COURSE CODE: 10B11EC612 MAX. MARKS: 50

COURSE NAME: VLSI TECHNOLOGY AND APPLICATIONS

COURSE CREDITS: 04 MAX. TIME: 2 HRS

Note: *All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means.*

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1. **[1 + 3 + 1 = 5]**

(a). What is the effect of scaling on gate capacitance? (Assume constant field scaling)

(b). Show width of channel, $C_{jsw,}$ and x_{ds} on the MOS structure.

(c). Write the formula showing body effect on linear and saturation region current equations for *n*-MOS.

2. Derive the equation for depth of depletion region. **[5]**

3. Prove threshold voltage is a function of substrate bias voltage. **[10]**

4. An *n*-channel device has $k_n` = 50\mu A/V^2$, $W/L = 20$ and $V_{th} = 0.8V$. The device is to operate as a switch for small V_{DS}, utilizing a control voltage V_{GS} in the range of 0V to 5V. Find the switch closure resistance r_{DS} and closure voltage V_{DS} obtained when $V_{GS} = 5V$ and $I_D = 1mA$. Recalling that $\mu_n = 0.4\ \mu_p$, what must *W/L* be for a *p*-channel device that provides the same performance as the *n*-channel device in this application? **[5]**

5. Draw and explain energy band diagram of all stages for *n*-MOS. **[10]**

6. Explain the device physics for an *n*-channel MOS transistor. Derive the current voltage relation in Linear region. **[10]**

7. Explain in detail about VLSI design cycle. **[5]**