JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

MAKE UP EXAMINATION- 2018

B.Tech VI Semester

COURSE CODE: 10B11EC612 **MAX. MARKS: 25**

COURSE NAME: VLSI TECHNOLOGY AND APPLICATIONS

COURSE CREDITS: 04 **MAX. TIME: 1 HR 30 MIN**

Note: *All questions are compulsory. Carrying of mobile phone during examinations will be treated as case of unfair means.*

1.

a. Give the relation between i_{DS}- v_{DS} of *p*-channel enhancement MOSFET in linear region.
b. Draw the symbol for *n*-channel depletion IGFET (show the substrate also).
c. Draw the Voltage Transfer Characteristic for resistive load *n*MOS inverter. Mark all critical voltages also.
d. What is channel length modulation? What is the effect of channel length modulation on current equation?
e. Draw energy band diagram for *n*-channel enhancement MOS for inversion layer.
f. Find the region of operation for *p*-MOS; V_{GS} = -3V, V_{DS} = -5V, V_{th} = -1.5V.
g. What is the formula for C_{GS} in linear mode for oxide related capacitance? Assume overlap length.
h. Give the formula where grading coefficient is used. Write its value for different types of junctions.

[CO1, CO3] [8 × 1 = 8]

2. a) Compare the two technology scaling methods. In particular, show analytically by using equations how the delay time, power dissipation per unit area, linear current, channel resistance, capacitance per unit area are affected in terms of the scaling factor S using any scaling method.

b) Draw the high frequency small signal model of a MOSFET. Write formulas of each parameter used in the model. **[CO2, CO3] [3.5 + 2.5 = 6]**

3. In an n-MOS transistor operating at room temperature following measurements are done: substrate doping density $10^{16}/cm^3$, gate oxide thickness = 400Å, source and drain diffusion doping density = $10^{17}/cm^3$, aspect ratio =5, gate to source voltage =4V, drain to source voltage = 4V, drain current =144μA, source to bias voltage = 2.6V. Find the threshold voltage, electron mobility, trans conductance, oxide related capacitance, and body effect. Assume oxide charge Q_{ox} and gate overlap is zero. **[CO1, CO3] [6]**

4. Calculate noise margins for resistive load inverter circuit with V_{DD} = 5V, $k`_n$ = 20μA/V^2, V_{T0} = 0.8V, R_L= 200KΩ, W/L = 2. Calculate the critical voltages. **[CO4] [5]**