JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -2 EXAMINATIONS-APRIL 2025

M.Tech-II Semester (ECE)

COURSE CODE (CREDITS): 21M11EC211 (3) MAX. MARKS: 25

COURSE NAME: Digital System Design using Verilog HDL

COURSE INSTRUCTOR: Dr. Pardeep Garg MAX. TIME: 1.5 Hours

Note: *(a) All questions are compulsory. (b) The candidate is allowed to make suitable numeric assumptions wherever required for solving problems.*

Q. No	Question	CO	Marks
Q1	*'A Full Adder (FA) can be designed using 2 half adders and an OR gate'* justify this statement depicting a logic diagram for the same. Write the Verilog HDL design code for such 1-bit FA using Gate-level modeling. The idea developed here can be extended to design a 4-bit Ripple Carry FA, draw the logic diagram for the same; and write the Verilog HDL design code for such 4-bit Ripple Carry FA using Gate-level modeling.	CO-2	1+1+1.5+1.5=5
Q2	In how many ways can the signals specified in the module instantiation and the ports declared in a module definition be connected? Discuss such methods in detail with their pros and cons.	CO-2	1.5+1.5=3

Q3	Corresponding to the Verilog design code and the stimulus code given below, sketch the input and output waveforms:
	
	// Design code
	module xnor_self (out, a,b);
	output out;
	input a,b;
	xnor #10 x1 (out,a,b);
	endmodule
	
	// Stimulus code
	
	module stimulus;
	reg A,B;
	wire OUT;
	xnor_self x2 (OUT, A, B);
	initial
	begin
	A=1'b0; B=1'b0;
		CO-3	3

	#10 A=1'b1; B=1'b1; #10 A= 1'b1; B=1'b0; #20 $finish; end endmodule		
Q4	The logical equality operators when operated on operands can yield an unknown (x) value whereas the case equality operators yield either 1 or 0 but never an unknown (x) value. Justify this statement using suitable examples.	CO-3	2.5
Q5	Using an appropriate number of test cases, differentiate between the bitwise and logical operators in terms of their working and subsequently the result obtained.	CO-3	2.5
Q6	In which situation Gate-level modeling works well and under what conditions Dataflow modeling is preferred over Gate-level modeling? Discuss it in detail with the proper justification.	CO-3	2
Q7	How is the conditional/ternary operator used in Verilog HDL? Discuss assuming any appropriate example by writing a Verilog code (design code only) in Dataflow modeling.	CO-2	2
Q8	Calculate the result of the following operations in Verilog HDL: i) Y = X<<2 for value of X = 4'b1011 ii) ~|A for the value of A = 4'b1010 iii) out = (3'b110, 3{A}, B[2]) for A=2'b01, B=3'b101 iv) M !== N for M = 4'b1zxx, N=4'b1zxz v) Y>=X for X = 4'b 1100, Y=4'b1101	CO-2	5